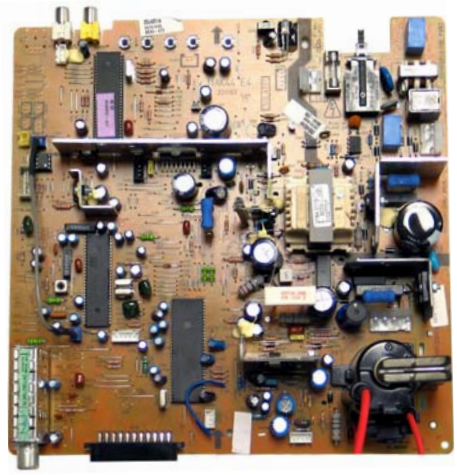
SHARP®

SERVICE MANUAL

SE00AK44CHA00
Issued: 9th March 2004

PAL B/G, I / SECAM L/L', B/G, D/K SYSTEM COLOUR TELEVISION



CHASSIS AK-44

In the interests of user safety (required by safety regulations in some countries) the set should be restored to its original condition and only parts identical to those specified should be used.

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SHARP CORPORATION

SERVICE MANUAL UPDATE LOG SHEET

Technical Report No. Technical Bulletin No.	Cause / Solution	Part No.	Page No.	Application Data /Serial No.

Use this page to keep any special servicing information as Technical Report (Bulletin), Technical Information, etc.
If only part number changes are required, just change part number directly the part number in the Parts Listing Section.
If you need more information, please refer to the Technical Report (Bulletin).

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SAFETY PRECAUTIONS

The service of this TV set must be carried out by qualified persons only. Components marked with the warning symbol on the circuit diagram or on the Parts Listing, are critical for safety and must only be replaced with an identical component.

- Power resistor and fused resistors must be mounted in an identical manner to the original component.
- When servicing this TV, check that the EHT does not exceed 26kV.

TV set switched off:

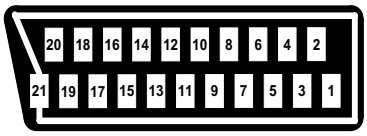
Make short-circuit between HV-CRT clip and CRT ground layer.
Short C809 before changing IC800 and IC801 or other components in primary side of the SMPS part.

Do not try to test Q801 gate source junction if C809 is charged, your meter will turn on the transistor which will discharge the capacitor resulting in a drain source short circuit. Do not discharge C809 quickly with a screwdriver etc. The very high current produced can damage the internal connections of the capacitor causing failure at a later date. Remember when checking voltages to use a return path on the same side of TR802 for the Voltmeter earth to obtain the correct readings.

Measurements:
Voltage readings and oscilloscope traces are measured under the following conditions:
Antenna signal's level is 60dB at the color bar pattern from the TV pattern generator. (100% white, 75% color saturation)
Brightness, contrast, and color are adjusted for normal picture performance.
Mains supply, 220VAC, 50Hz.

DO NOT CHANGE ANY MODULE UNLESS THE SET IS SWITCHED OFF
The mains supply part of the switch mode power supply's transformer is live.
Use an isolating transformer.
The receiver complies with the safety requirements.

PERI-TV SOCKET



SCART PINING
1 Audio right output 0.5 Vrms / 1K
2 Audio right input 0.5 Vrms / 10K
3 Audio left output 0.5 Vrms / 1K
4 Ground AF
5 Ground Blue
6 Audio left input 0.5 Vrms / 10K
7 Blue input 0.7 Vpp / 75 ohm
8 AV switching input 0-12 VDC / 10 K
9 Ground Green
10 -
11 Green input 0.7 Vpp / 75 ohm
12 -
13 Ground Red
14 Ground Blanking
15 Red input 0.7 Vpp / 75 ohm
16 Blanking input 0-0.4 VDC, 1-3 VDC / 75 Ohm
17 Ground CVBS output
18 Ground CVBS input
19 CVBS output 1 Vpp / 75 ohm
20 CVBS input 1 Vpp / 75 ohm
21 Ground

1. INTRODUCTION

11AK44 is a 90° chassis capable of driving 20"/21" tubes at the appropriate currents. The chassis is capable of operating in PAL, SECAM and NTSC standards. The sound system is capable of giving 4 watts RMS output into a load of 16 ohms. 7 page SIMPLETEXT is provided. The chassis is equipped with a single-deck 21 pin Scart connector.

CIRCUIT DESCRIPTIONS
2. SMALL SIGNAL PART WITH STV2248

STV2248 video processor is essential for realizing all small signal functions for a color TV receiver.

2.1 Vision IF amplifier

The vision IF amplifier can demodulate signals with positive and negative modulation. The PLL demodulator is completely alignment-free. Although the VCO (Toko-coil) of the PLL circuit is external, yet the frequency is fixed to the required value by the original manufacturer thus the Toko-coil does not need to be adjusted manually. The setting of the various frequencies (38.9 or 33,8 MHz) can be made via changing the coil itself.

2.2 QSS Sound circuit (QSS versions)

The sound IF amplifier is similar to the vision IF amplifier and has an external AGC de-coupling capacitor. The single reference QSS mixer is realised by a multiplier. In this multiplier the SIF signal is converted to the inter-carrier frequency by mixing it with the regenerated picture carrier from the VCO. The mixer output signal is supplied to the output via a high-pass filter for attenuation of the residual video signals. With this system a high performance hi-fi stereo sound processing can be achieved. The AM sound demodulator is realised by a multiplier. The modulated
sound IF signal is multiplied in phase with the limited SIF signal. The demodulator output signal is supplied to the output via a low-pass filter for attenuation of the carrier harmonics. The AM signal is supplied to the output via the volume control.

2.3 AM Demodulator

The AM demodulated signal results from multiplying the input signal by itself, it is available on AM/FM output.

2.4 FM demodulator and audio amplifier (mono versions)

The FM demodulator is realized as narrow-band PLL with external loop filter, which provides the necessary selectivity without using an external band-pass filter. To obtain a good selectivity a linear phase detector and constant input signal amplitude are required. For this reason the inter-carrier signal is internally supplied to the demodulator via a gain controlled amplifier and AGC circuit. The nominal frequency of the demodulator is tuned to the required frequency (4.5/5.5/6.0/6.5 MHz) by means of a calibration circuit that uses the clock frequency of the µ-controller/Teletext decoder as a reference. The setting to the wanted frequency is realized by means of the software. It can be read whether the PLL frequency is inside or outside the window and whether the PLL is in lock or not.
With this information it is possible to make an automatic search system for the incoming sound frequency. This is realized by means of a software loop that alternate the demodulator to various frequencies, then select the frequency on which a lock condition has been found. De-emphasis output signal amplitude is independent of the TV standard and has the same value for a frequency
deviation of ±25 kHz at the 4.5 MHz standard and for a deviation of ±50 kHz for the other standards. When the IF circuit is switched to positive modulation the internal signal on deemphasis pin is automatically muted. The audio control circuit contains an audio switch and volume control. In the mono inter-carrier sound versions the Automatic Volume Leveling (AVL) function can be activated. The pin to which the external capacitor has to be connected depends on the IC version. For the 90° types the capacitor is connected to the EW output pin (pin 20). When the AVL is active it automatically stabilizes the audio output signal to a certain level.

2.5 Video switching

The video processor (STV2248C) has three CVBS inputs and two RGB inputs. The first CVBS input is used for external CVBS from SCART 1, the second is used for external CVBS from FAV, and the third one is used for internal video. The selection between both external video inputs signals is realized by means of software and hardware switches.

2.6 Synchronization circuit

The video processor (STV224X) performs the horizontal and vertical processing. The external horizontal deflection circuit is controlled via the Horizontal output pulse (HOUT). The vertical scanning is performed through an external ramp generator and a vertical power amplifier IC controlled by the Vertical output pulse (VOUT).
The main components of the deflection circuit are:
• PLL1: the first phase locked loop that locks the internal line frequency reference on the CVBS input signal. It is

composed of an integrated VCO (12 MHz) that requires the chroma Reference frequency (4.43 MHz or 3.58 MHz crystal oscillator reference signal), a divider by 768, a line decoder, and a phase comparator.
• PLL2: The second phase locked loop that controls the phase of the horizontal output (Compensation of horizontal deflection transistor storage time variation). Also the horizontal position adjustment is also performed in PLL2.
• A vertical pulse extractor.
• A vertical countdown system to generate all vertical windows (vertical synchronization window, frame blanking pulses, 50/60 Hz identification window...).
• Automatic identification of 50/60 Hz scanning.
• PLL1 time constant control.
• Noise detector, video identification circuits, and horizontal coincidence detector.
• Vertical output stage including de-interlace function, vertical position control.
• Vertical amplitude control voltage output (combined with chroma reference output and Xtal 1 indication).

2.7 Chroma and luminance processing

The chroma decoder is able to demodulate PAL, NTSC and SECAM signals.
The decoder dedicated to PAL and NTSC sub-carrier is based on a synchronous demodulator, and an Xtal PLL locked on the phase reference signal (burst).
The SECAM demodulation is based on a PLL with automatic calibration loop.
The color standard identification is based on the burst recognition.
Automatic and forced modes can be selected through the I2C bus.
NTSC tint, and auto flesh are controlled through I2C bus.
Xtal PLL can handle up to 3 crystals to work in PAL M, PAL N and NTSC M for South America.
ACC an ACC overload control the chroma sub-carrier amplitude within 26dB range. Both ACCs are based on digital systems and do not need external capacitor.
All chroma filters are fully integrated and tuned via a PLL locked on Xtal VCO signal.
A second PLL is used for accurate fine-tuning of the SECAM bell filter. This tuning is achieved during the frame blanking. An external capacitor memorizes the bell filter tuning voltage.
A base-band chroma delay-line rebuilds the missing color line in SECAM and removes transmission phase errors in PAL.
The base-band chroma delay line is clocked with 6 MHz signal provided by the horizontal scanning VCO.
The luminance processor is composed of a chroma trap filter, a luminance delay line, a peaking function with noise coring feature, a black stretch circuit.
Trap filter and luminance delay lines are achieved with the use of bi-quad integrated filters, autoaligned via a master filter phase locked loop.

2.8 RGB output circuit

The video processor performs the R, G, B processing.
There are three sources:

1. Y, U, V inputs (coming from luma part (Y output), and chroma decoder outputs (R-Y, B-Y outputs).
2. External R, G, B inputs from SCART (converted internally in Y, U, V), with also the possibility to input YUV signals from a DVD player, (YUV specification is Y= 0.7 V PP , U= 0.7 V PP , V = 0.7 V PP for 100% color bar).
3. Internal R, G, B inputs (for OSD and Teletext display)

The main functions of the video part are:
- Y, U, V inputs with integrated clamp loop, allowing a DC link with YUV outputs,
- External RGB inputs (RGB to YUV conversion), or direct YUV inputs,
- Y, U, V switches,
- Contrast, saturation, brightness controls,
- YUV to RGB matrix,
- OSD RGB input stages (with contrast control),
- RGB switches,
- APR function,
- DC adjustment of red and green channels,
- Drive adjustments (R, G, B gain),
- Digital automatic cut-off loop control,
- Manual cut-off capability with I2C adjustments,
- Half tone, oversize blanking, external insertion detection, blue screen,
- Blanking control and RGB output stages.

2.9 µ-Controller

The ST92195 is the micro-controller, which is required for a color TV receiver. ST92195D1 is the version with one page Teletext and ST92195D7 is the one with 7 page Teletext. The IC has the supply voltage of 5 V and they are mounted in PSDIP package with 56 pins.

µ-Controller has the following features
- Display of the program number, channel number, TV Standard, analogue values, sleep timer, parental control and mute is done by OSD
- Single LED for stand-by and on mode indication
- System configuration with service mode
- 3 level logic output for SECAM and Tuner band switching

IC 501 controls all the functions of the receiver operated by the remote control and the front panel customer controls. It produces the on screen graphics, operates tuning, customers controls and engineering controls, and also incorporates all of the Teletext functions. It also controls the video processor, the audio processor, and the tuner. The circuits just mentioned are controlled via the I²C bus. Also IC501 controls the video source switching, vertical position adjustment and the vertical linearity adjustment via its ports.
An external 8K EEPROM is used by the micro. The EEPROM comes fully programmed. The main clock oscillator is 4.0 MHz crystal X501 on pins 50 and 51. Reset is provided on pin 2 via Q504. On switching on pin 2 becomes high and the controller gets reset which stays valid till a low signal comes on that pin.

2.9.1 Controls

Command information from the infrared remote controller is fed through the sensor IC502 to pin 1 of the micro-processor. Operation of the customer front panel keys is detected by pin 8 that is an ADC (analogue to digital converter). Pressing a switch will connect the 5V to the ground through a particular resistor that determines the value of the voltage on pin8 at that instant. This obtained value is comprehended by the micro and the corresponding operation is performed. Refer to the following table:

Button	Theoretical voltage	Resistance
P+	3.0V	R502
P-	4.0V	R503
V+	2.0V	R504
V-	1.5V	R506
Menu	1.0V	R505

IC501 automatically switches from TV mode to AV1 by detecting the signal from or pin8 at the Scart connector, through it 56 pins. The picture mode is determined according to the following table:

Direct Voltage	Picture mode
0 ~ 2 V	TV
4,5 ~ 7 V	16 :9
9,5 ~ 12 V	4 :3

2.9.2 Teletext

The microprocessor IC501 performs all of the Teletext functions internally. The Composite blanking video and Sync signal (CBVS) is input to pin 33 of the micro from pin 29 of IC403. When text is selected the text graphics are output as R.G.B signals on pins 15/16/17 of the micro and fed to pins 34/35/36 of IC403. At the same time pin 18 of the micro goes high taking pin 37 of IC403 high, blanking the picture and selecting text R.G.B. input.
Note: mixed mode is available and fast text with 8-page memory.

2.10 Video Path

The detected video signal is output from pins 18 of IC403, to sound traps Z403/404. The video is taken from the other side via the appropriate filter to Pin 18 of IC403. (1.2 p to p) Video to the Scart connectors is taken after R458 to Pin 19 of the Scart connector. The CVBS_TXT output Pin29 output is fed to IC501 Pin 34 (for Teletext). The video signal is sometimes labelled CVBS on the circuit diagram. This stands for Composite Video Blanking & Sync.
The composite signal is input Pin 13 (Video input) of IC403. This IC carries out all of the luma/Chroma processing internally and also provides the customer control functions of brightness, contrast, sharpness and saturation. IC403 is I²C bus controlled and incorporates auto greyscale circuitry and internal luma/chroma delay lines. The resulting R.G.B drive is output on pins 30,31 and 32. The R.G.B passes via connector PL405 to the CRT base PCB. Here the R.G.B signal is amplified by IC901 to provide drive for the cathodes of the CRT. IC901 produces a feedback signal, which is fed to IC403 (pin 33) for blanking and auto greyscale correction.

2.11 Sound Path

The demodulated mono sound is taken from pin 55 of IC403 directly to the sound output stage IC401 Pin 7. The output signal from IC401 is Volume controlled achieved within IC403 using the I²C bus line from IC501. To limit the volume at the specified out put the A_out pin 55 is fed to IC 401 through a voltage divider R455 and R454. Muting of the output stage is provided from Pin 46 of IC501 to pin3 of IC401/6 of IC301.
IN the stereo model the IF from PINS 10 & 11 of the tuner passes through Z401 and the output signal goes through pins 1&2 of IC403. The output QSS signal from IC 403 is taken from pin 11 and sent to audio processor IC700. The left channel is output on PIN 29 and the right channel output is on PIN 28. Then to IC301 after passing through a voltage divider R454/R455 for the right channel and R463/R464 for the left channel.
IC403 handles also the AM modulated signals in L/L' systems at pins 1&2.

2.12 AV Input Signal Path

2.12.1 Video and Sound

IC403 has three CVBS inputs at pins 18,20 and 22.The composite video signal of AV1 is taken from pin 20 of the Scart connector to pin 20 of IC403. The mono sound signal is taken from pins 2 and 6 of the Scart sockets to the switching transistors Q101. The transistor switches the audio depending on the source, and is then fed to pin14 of IC403.
When AV input is selected pin 5,6,7 of the microprocessor IC50I is taken high, this switches the IC403 to external input mode via I²C BUS. This connects the video inputs on pins 20 or 22 to IC403 and the audio input on pin 14 to the audio out on pin 55 (via the internal volume control circuit) The signal paths are then as for videopath.
The chassis can detect the video signals on Scart using pin 8 switching voltage at pin 56 of IC501.

2.12.2 R.G.B

The R.G.B signals from pins 7,11 and 15 of the Scart connector are fed to the R.G.B input pins (25,26,27) of IC403.
R.G.B operation can be enabled by either taking pin 16 of the Scart connector high, this high is fed to Pin 28 of IC403, or via the I²C bus the microprocessor sets IC403 to forced R.G.B mode in which the video processor generates its own fast blank signal. This puts the IC into external R.G.B mode and selects the inputs on pins 25,26 and 27, overriding the video input on pin 20/22.
Note: when using R.G.B input the contrast, brightness and colour controls will still operate.

3. TUNER

Either a PLL or a VST tuner is used as a tuner.
UV1316 (VHF/UHF) is used as a PLL tuner. For only PALM/N, NTSC M applications UV 1336 is used as the PLL tuner. UV 1315 (VHF/UHF) is used as a VST Tuner.

Channel coverage of UV1316

BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
	CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
Low Band	E2 to C	48.25 to 82.25 **(1)**	S01 to S08	69.25 to 154.25
Mid Band	E5 to E12	175.25 to 224.25	S09 to S38	161.25 to 439.25
High Band	E21 to E69	471.25 to 855.25 **(2)**	S39 to S41	447.25 to 463.25

(1). Enough margin is available to tune down to 45.25 MHz.

(2). Enough margin is available to tune up to 863.25 MHz.

Noise	Typical	Max.	**Gain**	Min.	Typical	Max.
Low band:	5 dB	9 dB	All channels:	38 dB	44 dB	52 dB
Mid band:	5dB	9 dB	Gain Taper (of-air channels):			8 dB
High band:	6 dB	9 dB				

Channel Coverage UV1336

BAND	CHANNELS	FREQUENCY RANGE (MHz)
Low Band	2 to D	55.25 to 139.25
Mid Band	E to PP	145.25 to 391.25
High Band	QQ to 69	397.25 to 801.25

Noise is typically 6 dB for all channels. **Gain** is minimum 38 dB and maximum 50 dB for all channels.

Channel Coverage of UV1315

BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
	CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
Low Band	E2 to C	48.25 to 82.25 **(1)**	S01 to S10	69.25 to 168.25
Mid Band	E5 to E12	175.25 to 224.25	S11 to S39	231.25 to 447.25
High Band	E21 to E69	471.25 to 855.25 **(2)**	S40 to S41	455.25 to 463.25

(1). Enough margin is available to tune down to 45.25 MHz.
(2). Enough margin is available to tune up to 863.25 MHz.

Noise	Typ.	Max.	**Gain**	Min.	Typ.	Max.
Low band	6 dB	9 dB	All Channels	38 dB	44 dB	50 dB
Mid band	6 dB	10 dB	Gain Taper			8 dB
High band	6 dB	11 dB	(off-air channels)			

4. DIGITAL TV SOUND PROCESSOR MSP34X0

The MSP 34x0G is designed to perform demodulation of FM or AM-Mono TV sound.
Alternatively, two-carrier FM systems according to the German or Korean terrestrial specs or the satellite specs can be processed with the MSP 34x0G. Only the MSP 3410 does digital demodulation and decoding of NICAM-coded TV stereo sound. The MSP 34x0G offers a powerful feature to calculate the carrier field strength which can be used for automatic standard detection (terrestrial) and search algorithms (satellite).

5. SOUND OUTPUT STAGE TDA7266L/TDA7266

TDA7266L is used as the AF output amplifier for mono applications. It is supplied by +12 VDC coming from a separate winding in the SMPS transformer. An output power of 4 W (THD = 0.5 %) can be delivered into an 16 ohm load.
TDA7266 is used as the AF output amplifier for stereo applications. It is supplied by +12 VDC coming from a separate winding in the SMPS transformer. An output power of 2*4W (THD = 0.5 %) can be delivered into an 16 ohm load.

6. VERTICAL OUTPUT STAGE WITH TDA8174A

The TDA8174A is a power amplifier circuit for use in 90° and 110° color deflection systems for 25 to 200 Hz field frequencies, and for 4 : 3 and 16 : 9 picture tubes.
IC403 generates a vertical pulse signal VER_OUT and V_AMP that are fed to IC600 (the vertical stage IC). IC600 is supplied by a 26V DC via diode D610. It generates its own ramp signal and based on the V_AMP & VER_OUT signals it produces the vertical deflection signals that are fed to connector PL601. Vertical linearity adjustment is controlled by Q604, which is driven by the PWM output of IC501 at pin 49. Vertical position adjustment is conducted by Q606 derived by the VER_OUT signal. Switching Q606 will change the DC voltage on VOUT_2 pin, which will either lower or higher the picture. A DC level is supplied at VOUT_2 via D614 to stabilise the picture and make its position changeable.

7. VIDEO OUTPUT AMPLIFIER TDA6107JF/N3

The TDA6107JF includes three video output amplifiers and is intended to drive the three cathodes of a colour CRT directly. The device is contained in a plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package, and uses high-voltage DMOS technology. To obtain maximum performance, the amplifier should be used with black-current control.

8. POWER SUPPLY (SMPS)

The DC voltage required at various parts of the chassis are provided by an SMPS transformer controlled by the IC MC44608 which is designed for driving, controlling and protecting switching transistor of SMPS. The transformer produces 126 V (Flat models) or 116 V (non Flat models) for FBT input, +/- 14 V for audio output IC, S + 3.3, S + 5 V and 8 V for ST92195.

The ZX series of receivers incorporate a Motorola switch mode power supply using a MC 44608 regulator controller IC. The circuit provides power to the receiver in both standby and normal operation modes.

8.1 Start Up

The switch on the mains supply is fed through the mains filter network TR801, the surge limiter resistor *R828,* the bridge rectifier diodes *D811/13/37/38,* and reservoir capacitor producing approx. 320 volts D.C. to feed the switching MOSFET Q801 via the primary winding of TR802 pins 6 and 7.

Start up resistor R801 feeds from a 500V coming from the mains through the adder diodes D809, D890 to pin 8 of IC800, the IC uses 9mA current source and connects it internally to VCC at pin6 allowing a rapid charge enough for start up. Then IC800 responds with the oscillator starting to oscillate at a 40 KHz frequency fixed by the IC manufacturer.

The IC then produces, pulse width modulation pulses, at this frequency on pin 5 to drive the base of the switching FET Q801, that will then switch current on and off through the primary of TR802, which will in turn provides voltages in the secondary windings. The secondary winding voltages being proportional to the length of time that Q801 is turned on in each cycle. The voltage produced between pins 4 and 3 of TR802 is rectified by D804 developing aprox. 12 volts on C810, which takes over from the start up resistor to supply pin 8 of IC800.

The Demag pin at pin1 offers 3 different functions: Zero voltage crossing detection (50mV), 24mA current detection and 120mA current detection. The 24mA level is used to detect the secondary reconfiguration status and the 120mA level to detect an Over Voltage status called Quick OVP.

The VCC at pin6 operates between 6,6V and 13V in normal operation, when this voltage exceeds 15V then the IC output is disabled.

8.2 Voltage Regulation

After initial start up the secondary voltages of TR802 are established. These voltages then need to be regulated to the required levels. In a switch mode power supply such as this, it is the ON time of the switching FET Q801 that determines the output voltages produced. To provide regulation of the supply there is a feedback loop via an adjustable zener IC118 and an OPTO- coupler connected to pin3 of IC800. The reference voltage of IC118 is set to 2,5V to supply a B+ voltage of 115V. Any fluctuation at this pin will cause IC800 to compensate it either by increasing or decreasing the voltage at the secondary outputs.

8.3 Voltage Protection

The MC44608 offers two OVP functions:

1- A fixed function that detects when V CC is higher than 15.4V

2- A programmable function that uses the demag pin. The current flowing into the demag pin is mirrored and compared to the reference current Iovp (120mA). -Thus this OVP is quicker than normal number one as it directly senses the change in current rather than waiting for a specific voltage value, and is called QOVP. In both cases, once an OVP condition is detected, the output is latched off until a new circuit START–UP.

3- A software controlled function acts on pin52 of IC501. This pin monitors feedback from both 8V and 5V via D512, then compares these to a reference value Vref pre-set by the hardware through resistors R545, R546, R548. In normal mode operation 1.2V < Vref < 2.4V. Any voltage outside this window will cause the micro controller to force the TV to stand by mode by lowering the standby port. Refer to standby mode.

8.4 Current Protection

To monitor the current drawn by the receiver the source of Q801 is returned to the bridge rectifier through a low value resistor R807. All the current drawn by the receiver will flow through that resistor each time Q801 conducts; this will produce a voltage across the resistors proportional to the current drawn by the receiver. This voltage is fed to pin 2 of IC800 via R806. When the receiver is working normally the voltage across R807 is only a fraction of a volt and is not large enough to have any effect on IC800. Under fault conditions, if the receiver draws excessive current the voltage across *R807* will rise. This voltage is monitored by the current sense input pin2.

This Current Sense pin senses the voltage developed on the series resistor R806 inserted in the source of the power MOSFET. When I sense reaches 1V, the Driver output (pin 5) is disabled. This is known as the Over Current Protection function. A 200mA current source is flowing out of the pin 3 during the start–up phase and during the switching phase in case of the Pulsed Mode of operation. A resistor can be inserted between the sense resistor and the pin 3, thus a programmable peak current detection can be performed during the SMPS stand–by mode.

8.5 Standby Operation

As mentioned earlier the Start–up Management of MC44608 is as follows:
The Vi pin 8 of IC800 is directly connected to the HV DC rail Vin. This high voltage current source is internally connected to the VCC pin and thus issued to charge the VCC capacitor. The V CC capacitor charge period corresponds to the Start–up phase. When the V CC voltage reaches 13V, the high voltage 9mA current source is disabled and the device starts working. The device enters into the switching phase.
To help increase the application safety against high voltage spike on pin8 a small wattage 1k _ series resistor is inserted between the Vin rail and pin 8. After this start-up the IC can distinguish between the different modes of operation using the following technique:

8.6 Mode Transition

The LW latch is the memory of the working status at the end of every switching sequence. Two different cases must be considered for the logic at the termination of the SWITCHING PHASE:
1. No Over Current was observed
2. An Over Current was observed

These two cases correspond to the two signals “NOC” in case of “No Over Current” and “OC” in case of Over Current. The effective working status at the end of the ON time memorized in LW corresponds to Q=1 for no over current, and Q=0 for over current.
To enter the standby mode secondary side is reconfigured using D889 loop, this starts with the microprocessor ‘s pin 47 becomes high; as the standby port becomes high Q503 conducts and Q802 becomes off then D889 conducts and the high voltage output value becomes lower than the NORMAL mode regulated value. The shunt regulator IC118 is fully OFF. In the SMPS stand–by mode all the SMPS outputs are lowered except for the low voltage output that supply the wake–up circuit located at the isolated side of the power supply. In that mode the secondary regulation is performed by the Zener diode (D801) connected in parallel to the TL431. The secondary reconfiguration status can be detected on the SMPS primary side by measuring the voltage level at pin4 of TR802.
In the SMPS stand–by mode the 3 distinct phases are:
The SWITCHING PHASE: Similar to the Overload mode. The current sense clamping level is reduced. When VCC crosses the current sense section, the C.S. clamping level depends on the power to be delivered to the load during the SMPS stand–by mode. Every switching sequence ON/OFF is terminated by an OC as long as the secondary Zener diode voltage has not been reached. When the Zener voltage is reached the ON cycle is terminated by a true PWM action. The proper SWITCHING PHASE termination must correspond to a NOC condition. The LW latch stores this NOC status. The LATCHED OFF PHASE: The MODE latch is set.
The START–UP PHASE is similar to the Overload Mode. The MODE latch remains in its set status (Q=1).
The SWITCHING PHASE: The Stand-by signal is validated and the 200uA is sourced out of the Current Sense pin 2.

8.7 SMPS Switch Off

When the mains is switched OFF, so long as the electrolytic bulk capacitor provides energy to the SMPS the controller remains in the switching phase. Then the peak current reaches its maximum peak value, the switching frequency decreases and all the secondary voltages are reduced. The V CC voltage is also reduced. When VCC is less than 6,5V, the SMPS stops working

9. LINE CIRCUIT

Line and frame drive are generated by IC403. The sync pulses are separated from the incoming video signal at pin 18/ 20/22 and used to control the internal circuitry of the IC. Line drive is produced by counting down the external 4.43 MHz crystal at pin 40 to 15.625 KHz locked to the incoming sync. This drive is output on pin 48 and feeds directly to the line drive transistor Q601. Note. That the output of IC403 Pin 48 is an open-collector and requires a pull up resistor, if the pin is open circuited for test no waveform will be seen. Q601 collector feeds the line output transistor Q603.
The line output stage is conventional with a transformer containing a split diode winding for EHT generation. Fifth harmonic tuning is achieved by capacitor C618/619.
A fly-back pulse is taken from pin 1 of the FBT transformer. This is required by IC403 (Pin 49) for burst / sync gating, and RGB line blanking. The ver_sync signal is output from the pin47 and fed to Pin41 of IC501. The H_sync pulse is taken from pin 1 of the FBT and fed to the micro at pin 40. These two signals are required by the micro for graphics timing and also for text.

9.1 B.C.L Circuit (Beam Current Limiter)

Beam current limiting is employed to protect the circuitry in the receiver, the CRT and to prevent excessive X Ray radiation in fault conditions. The current drawn by the CRT is monitored by the current drawn through the winding of the fly-back transformer that produces the EHT for the CRT anode. The end of the winding (Pin 10) is returned to IC403 Pins 46, the beam current drawn by the CRT passes through Q603 and develops a voltage on the collector proportional to the current (V=IxR).

The voltage on the collector will vary depending on the beam current being drawn reducing the brightness and contrast of the picture. If the voltage is sufficiently negative (indicating very high excess beam current) the output will be reduced, reducing the picture brightness and contrast.

10. SERIAL ACCESS CMOS 8K EEPROM 24C08

The 24C08 is a 8 Kbit electrically erasable programmable memory (EEPROM), organized as 4 blocks of 256*08 bits. The memory is compatible with the I²C standard, two wire serial interface which uses a bi-directional data bus and serial clock.

EEPROM Initialisation

If the E²PROM IC500 is replaced it will come fully programmed and therefore it is not necessary to initialise the new device. In some circumstances the E²PROM may become corrupted in use i.e. static discharge or lightning strike. If this happens, it is advised that the E²PROM is replaced.

11. SAW FILTERS

Saw filter type: Model:
G1975M: PAL B/G MONO
K2966M: PAL SECAM B/G/D/K/I MONO
J1981 : PAL-I MONO
K2958M: PAL-SECAM B/G-D/K (38) MONO
2962M: PAL-SECAM B/G/D/K/I/L/L' MONO
L9653M: SECAM L/L' AM MONO (AUDIO IF)
G3967M: PAL-SECAM B/G STEREO (VIDEO IF)
G9353M: PAL-SECAM B/G STEREO (AUDIO IF)
K3958M: PAL-SECAM B/G/D/K/I/L/L' STEREO (VIDEO IF)
K9356M: PAL-SECAM B/G/D/K/I STEREO (AUDIO IF)
K9656M: PAL-SECAM B/G/D/K/I/L/L' STEREO (AUDIO IF)
K3958M: PAL I NICAM (VIDEO IF)
K9356M: PAL I NICAM (AUDIO IF)

12. IC DESCRIPTIONS AND INTERNAL BLOCK DIAGRAM

ST92195
STV224X
TUNER (UV1315, UV1316, UV1336)
TDA7266L / TDA7266M
TDA8174A
TDA6107
MC44608
MSP34X0G
24C08
TDA1308
SAW FILTERS
G1975M, K2966M, K2962M, L9653M, G3962M, G9353M, K3958M, K9356M, K9656M, K6263K, K9652M

ST92195

The ST92195 is a member of the ST9+ family of micro-controllers, completely developed and produced by STMicroelectronics using a proprietary n-well HCMOS process. The nucleus of the ST92195 is the advanced Core, which includes the Central Processing Unit (CPU), the ALU, the Register File and the interrupt controller. The Core has independent memory and register buses to add to the efficiency of the code. A set
of on-chip peripherals form a complete system for TV set and VCR applications:

– Voltage Synthesis
– VPS/WSS Slicer
– Teletext Slicer
– Teletext Display RAM
– OSD

Additional peripherals include a watchdog timer , a serial peripheral interface (SPI), a 16-bit timer and an A/D converter.

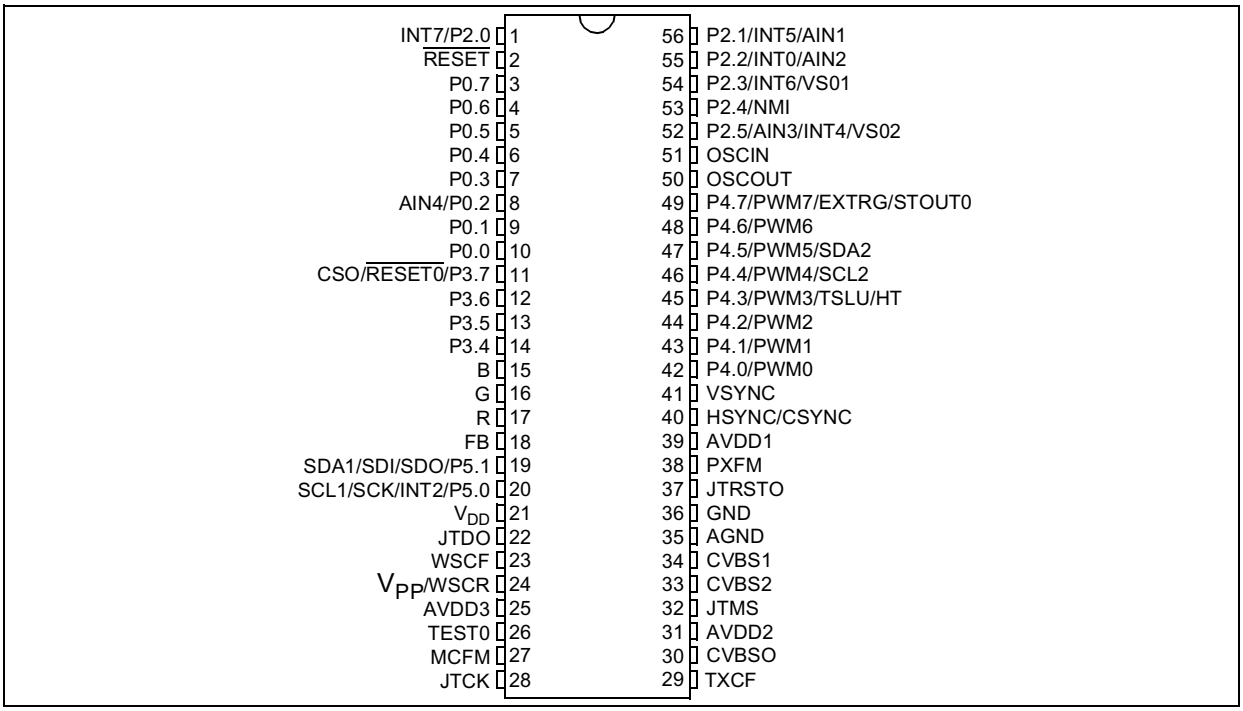


Figure 1. Microcontroller Pin Description

STV224X Video processor

The STV2246/2247/2248 are fully bus controlled ICs for TV including PIF, SIF, luma, Chroma and deflection processing. Used with a vertical frame booster (TDA1771 or TDA8174 for 90° chassis, STV9306 for 110° chassis), they allow the design of multi-standard sets with very few external components and no manual adjustments.

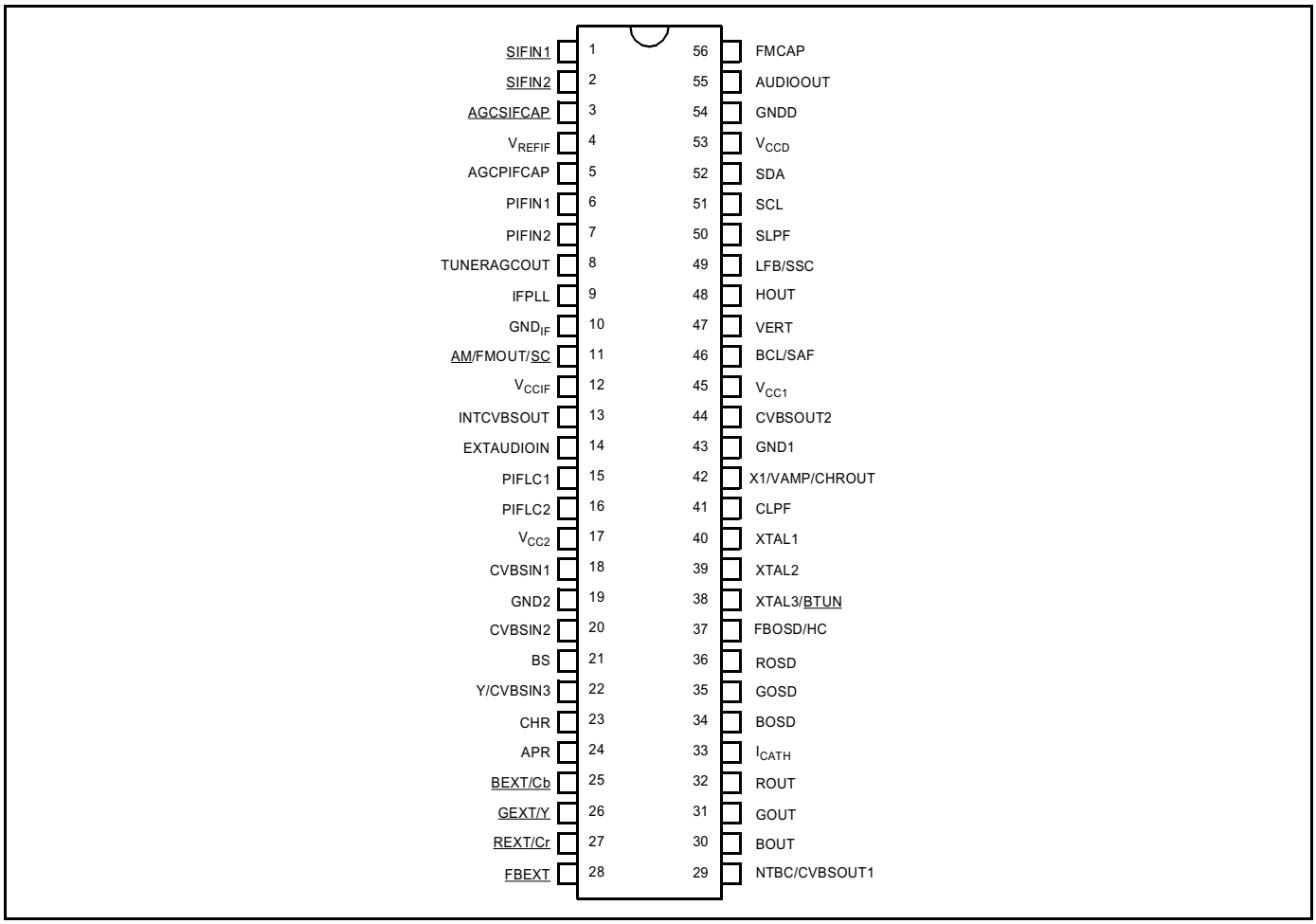


Figure 2. Pin connections STV224X/8X (SDIP56)

UV1315, UV1316, UV1336

General description of UV1315

The UV1315 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'.

Features of UV1315

Member of the UV1300 family small sized UHF/VHF tuners
Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
Voltage synthesized tuning (VST)
Off-air channels, S-cable channels and Hyper-band
Standardized mechanical dimensions and pinning

Pinning, Pin Value

1. Gain control voltage (AGC): 4.0 V, Max: 4.5 V
2. Tuning voltage
3. High band switch: 5 V, Min: 4.75 V, Max: 5.5 V
4. Mid band switch: 5 V, Min: 4.75 V, Max: 5.5 V
5. Low band switch: 5 V, Min: 4.75 V, Max: 5.5 V
6. Supply voltage: 5 V, Min: 4.75 V, Max: 5.5 V
7. Not connected

8. Not connected
9. Not connected
10. Symmetrical IF output 1
11. Symmetrical IF output 2

Band switching table:

	Pin 3	Pin 4	Pin 5
Low band	0 V	0 V	+ 5 V
Mid band	0 V	+ 5 V	0 V
High band	+ 5 V	0 V	0 V

General description of UV1316

The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'.

Features of UV1316

Member of the UV1300 family small sized UHF/VHF tuners
Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
Digitally controlled (PLL) tuning via I²C-bus
Off-air channels, S-cable channels and Hyper-band
World standardized mechanical dimensions and world standard pinning
Complies to "CENELEC EN55020" and "EN55013"

Pinning, Pin Value

1. Gain control voltage (AGC): 4.0 V, Max: 4.5 V
2. Tuning voltage
3. I²C-bus address select: Max: 5.5 V
4. I²C-bus serial clock :Min: -0.3 V, Max: 5.5 V
5. I²C-bus serial data :Min: -0.3 V, Max: 5.5 V
6. Not connected
7. PLL supply voltage: 5.0 V, Min: 4.75 V, Max: 5.5 V
8. ADC input
9. Tuner supply voltage: 33 V, Min: 30 V, Max: 35 V
10. Symmetrical IF output 1
11. Symmetrical IF output 2

General description of UV1336

UV1336 series is developed for reception of channels broadcast in accordance with the M, N standard.

Features of UV1336

Global standard pinning
Integrated Mixer-Oscillator & PLL function
Conforms to CISPR 13, FCC and DOC (Canada) regulations
Low power consumption
Both Phono connector and 'F' connector are available

Pinning, Pin Value

1. Gain control voltage: 4.0 V, Max: 4.5 V
2. Tuning voltage
3. Address select Max: 5.5 V
4. Serial clock: Min: -0.3 V, Max: 5.5 V
5. Serial data :Min: -0.3 V, Max: 5.5 V
6. Not connected
7. Supply voltage: 5.0 V, Min: 4.75 V, Max: 5.5 V
8. ADC input (optional)
9. Tuning supply voltage: 33 V, Min: 30 V, Max: 35 V
10. Ground
11. IF output

TDA7266/TDA7266L

General Description of TDA7266L

The TDA7266L is a mono bridge amplifier specially designed for TV and Portable Radio applications. Requires very few external components

WIDE SUPPLY VOLTAGE RANGE (3-18 V)
MINIMUM EXTERNAL COMPONENTS.
– NO SVR CAPACITOR
– NO BOOTSTRAP
– NO BOUCHEROT CELLS
– INTERNALLY FIXED GAIN
STAND-BY & MUTE FUNCTIONS
SHORT CIRCUIT PROTECTION
THERMAL OVERLOAD PROTECTION

Pinnig

1 N.C.
2 N.C.
3 MUTE
4 ST-BY
5 PW-GND
6 S-GND
7 IN
8 VCC
9 OUT+
10 OUT -

General Description of TDA7266

The TDA7266 is a 2x7 Watt dual power amplifier. It is used for sound amplification at stereo TV sets.

WIDE SUPPLY VOLTAGE RANGE (3-18 V)
MINIMUM EXTERNAL COMPONENTS
– NOSWR CAPACITOR
– NOBOOTSTRAP
– NO BOUCHEROT CELLS
– INTERNALLY FIXED GAIN
STAND-BY & MUTE FUNCTIONS
SHORT CIRCUIT PROTECTION
THERMAL OVERLOAD PROTECTION

Pinnig

1. OUT1 +
2. OUT1 –
3. VCC
4. IN1
5. N.C.
6. MUTE
7. ST-BY
8. PW-GND
9. S-GND
10. N.C.
11. N.C.
12. IN2
13. VCC
14. OUT2 -
15. OUT2 +

TDA8174AW

INDEPENDENT VERTICAL AMPLITUDE ADJUSTMENT. BUFFER STAGE. POWER AMPLIFIER.
FLYBACK GENERATOR. THERMAL PROTECTION. INTERNAL REFERENCE VOLTAGE DECOUPLING.

General Description
TDA8174A and TDA8174AW are a monolithic integrated circuits. It is a full performance and very efficient vertical deflection circuit intended for direct drive of a TV picture tube in Color and B & W television as well as in Monitor and Data displays.

Pinning
1. POWER OUTPUT
2. OUTPUT STAGE Vs
3. TRIGGER INPUT
4. HEIGHT ADJUSTMENT
5. VOLTAGE REF DECOUPLING
6. GROUND
7. RAMP GENERATOR
8. BUFFER OUTPUT
9. INVERTING INPUT
10. Vs
11. FLYBACK GENERATOR

TDA6107

Features
- · Typical bandwidth of 5.5 MHz for an output signal of 60 V (p-p)
- · High slew rate of 900 V/ms
- · No external components required
- · Very simple application
- · Single supply voltage of 200 V
- · Internal reference voltage of 2.5 V
- · Fixed gain of 50
- · Black-Current Stabilization (BCS) circuit with voltage window from 1.8 to 6 V and current window from -100 mA to 10 mA
- · Thermal protection
- · Internal protection against positive flashover discharges appearing on the CRT.

General Description

The TDA6107JF includes three video output amplifiers and is intended to drive the three cathodes of a colour CRT directly. The device is contained in a plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package, and uses high-voltage DMOS technology. To obtain maximum performance, the amplifier should be used with black-current control.

Pinning, Pin Value
1. BLUE INPUT
2. VCC LOW VOLTAGE
3. GREEN INPUT
4. RED INPUT
5. VDD HIGH VOLTAGE
6. RED CATHODE CURRENT
7. RED OUTPUT
8. GROUND
9. RED FEEDBACK
10. GREEN OUTPUT
11. GREEN CATHODE CURRENT
12. GREEN FEEDBACK
13. BLUE OUTPUT
14. BLUE CATHODE
15. BLUE FEEDBACK

MC44608

General description
The MC44608 is a high performance voltage-mode controller designed for off–line converters. This high voltage circuit that integrates the start–up current source and the oscillator capacitor, requires few external components while offering a high flexibility and reliability.
The device also features a very high efficiency stand–by management consisting of an effective Pulsed Mode operation. This technique enables the reduction of the stand–by power consumption to approximately 1 W while delivering 300 mW in a 150 W SMPS.

- Integrated start–up current source
- Loss less off–line start–up
- Direct off–line operation
- Fast start–up

General Features
- Flexibility
- Duty cycle control
- On chip oscillator switching frequency 40, or 75 KHz
- Secondary control with few external components

Protections
- Maximum duty cycle limitation
- Cycle by cycle current limitation
- Demagnetization (Zero current detection) protection
- “Over V CC protection” against open loop
- Programmable low inertia over voltage protection against open loop
- Internal thermal protection

GreenLine Controller
- Pulsed mode techniques for a very high efficiency low power mode
- Lossless start-up
- Low dV/dT for low EMI radiation

Pinning, Pin Value
1. Demagnetization Zero cross detection voltage: 50 mV typ.
2. I Sense Over current protection voltage 1 V typ.
3. Control Input Min: 7.5 V Max.: 18 V
4. Ground Iout 2 Ap-p during scan 1.2 Ap-p during flyback
5. Driver Output resistor 8.5 Ohm sink 15 Ohm source typ.
6. Supply voltage Max: 16 V (Operating range 6.6 V - 13 V)
7. No connection
8. Line Voltage Min: 50 V Max: 500 V

MSP34X0G

The MSP 34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 3 shows a simplified functional block diagram of the MSP 34x0G. This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.
Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard. Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x0G has optimum stereo performance without any adjustments. All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x0G further simplifies controlling software.
Standard selection requires a single I2C transmission only. The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection).

Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/ stereo/bilingual; no I2C interaction is necessary (Automatic Sound Selection). The MSP 34x0G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China. The ICs are produced in submicron CMOS technology.

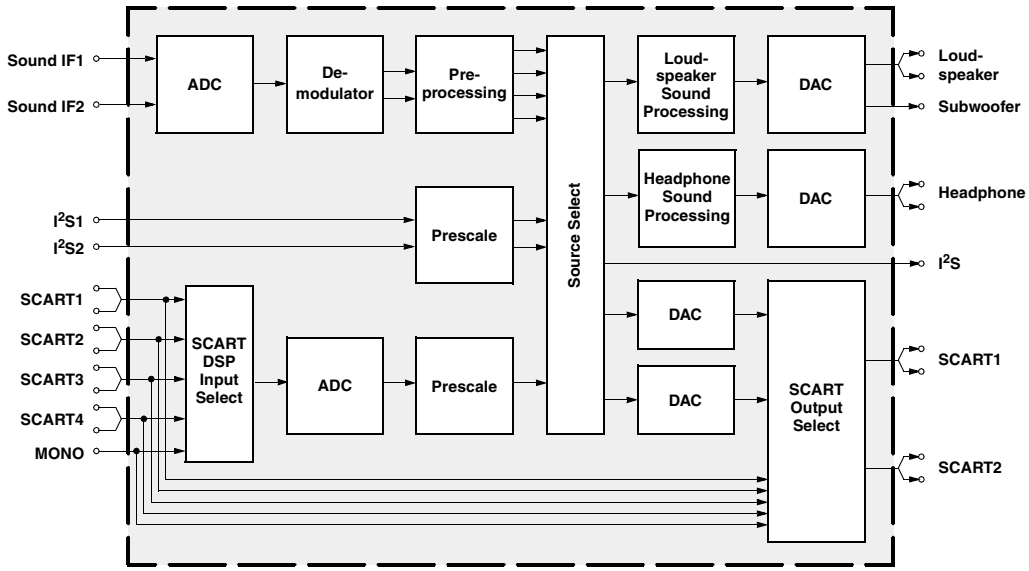


Figure 3. Simplified functional block diagram of the MSP 34x0G.

24C08

General description
The 24C08 is a 8 Kbit electrically erasable programmable memory (EEPROM), organized as 4 blocks of 256 * 08 bits. The memory operates with a power supply value as low as 2.5 V.

Features

Minimum 1 million ERASE / WRITE cycles with over 10 years data retention
Single supply voltage: 4.5 to 5.5 V
Two wire serial interface, fully I²C-bus compatible
Byte and Multi-byte write (up to 8 bytes)
Page write (up to 16 bytes)
Byte, random and sequential read modes
Self timed programming cycle

Pinning, Pin Value

1. Write protect enable: 0 V
2. Not connected: 0 V
3. Chip enable input: 0 V
4. Ground: 0 V
5. Serial data address input/output: Input LOW voltage: Min: -0.3 V, Max: 0.3 * Vcc: Input HIGH voltage: Min: 0.7* Vcc, Max: Vcc+1
6. Serial clock: Input LOW voltage: Min: -0.3 V, Max: 0.3 * Vcc: Input HIGH voltage: Min: 0.7 * Vcc, Max: Vcc+1
7. Multibyte/Page write mode: Input LOW voltage: Min: -0.3 V, Max: 0.5 V: Input HIGH voltage: Min: Vcc - 0.5, Max: Vcc + 1
8. Supply voltage: Min: 2.5 V, Max: 5.5 V

TDA1308

Features

Wide temperature range
Excellent power supply ripple rejection
Low power consumption
Short-circuit resistant
High performance
high signal-to-noise ratio
low distortion

Pinning, Pin Value

1. Output A (Voltage swing): Min: 0.75 V, Max: 4.25 V
2. Inverting input A: Vo (clip): Min: 1400 mVrms
3. Non-inverting input A: 2.5 V
4. Ground: 0 V
5. Non-inverting input B: 2.5 V
6. Inverting input B: Vo (clip): Min: 1400 mVrms
7. Output B (Voltage swing): Min: 0.75 V, Max: 4.25 V
8. Positive supply: 5 V, Min: 3.0 V, Max: 7.0 V

Saw filter's list

		VIDEO	AUDIO
MONO	PAL BG	G1975M	
	PSBG DK	K2966M	
	PAL II'	J1981	
	PSBGDKK' II'	K2966M	
	PSBGDKK' LL'	K2962M	L9653

		VIDEO	AUDIO
STR	PAL BG	G3967M	G9353M
	PAL II'	K3958M	K9356
	PSBGDKK' II'	K3958M	K9356
	PSBGDKK' LL'	K3958M	K9656

Pinning

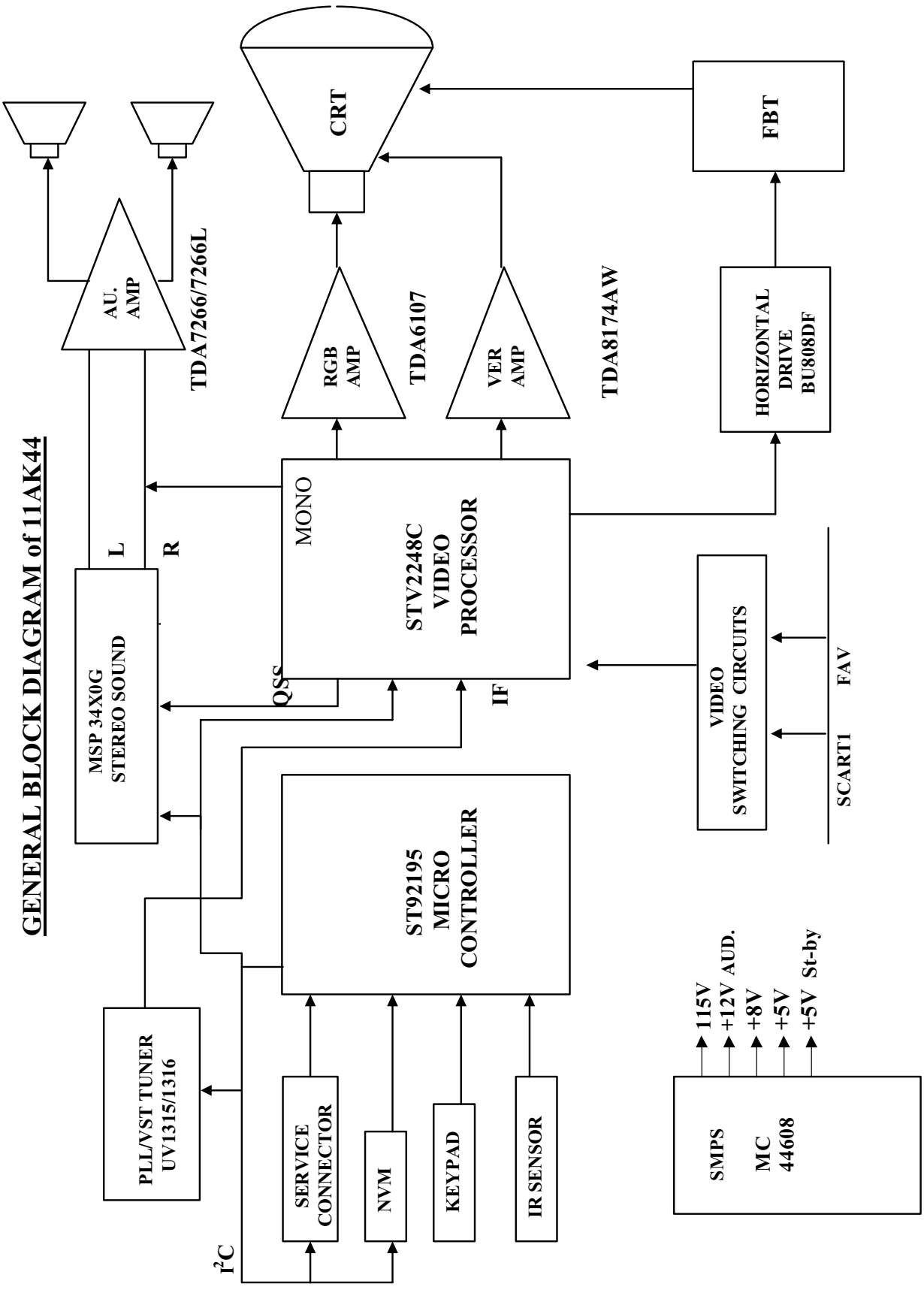
1. Input
2. Input-ground
3. Chip carrier-ground
4. Output
5. Output

K9656M, L9653M

Pinnig

1. Input
2. Switching Input
3. Chip carrier-ground
4. Output
5. Output

13. GENERAL BLOCK DIAGRAM of 11AK44



14. SERVICE MENU

14.1 Service Menu entrance

All system, geometry and white balance alignments are performed in Service Mode. Before starting the service mode alignments, make sure that all manual adjustments are done correctly.

To enter the service mode:
1. Press the MENU (30) button on the remote control gun. See figure 5.
2. Press digit keys 4, 7, 2 and 5 consecutively.

When the Service Mode is entered the following On Screen Display appears (figure 4):

Figure 4. Service Mode

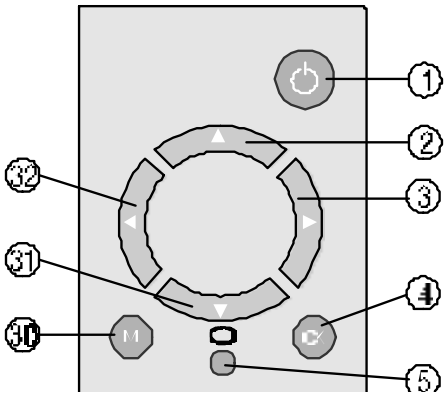


Figure 5. Remote Control

To adjust the different registers:
1. Use the CURSOR UP (2) / DOWN (31) buttons to move between the registers. See the above right figure.
2. Use the CURSOR LEFT (32) / RIGHT (3) buttons to change the data. See figure 5.

To memorize the adjustment:
It is not required to memorize the adjustment. Data are stored automatically.

To exit the Service Mode:
Switch the TV off using the mains switch.

14.2 Service Adjustments

Register	Parameter	Notes	Default Values	
			A51EFS13X191	A51ELD032X001
OSD	OSD Horizontal Position		70	81
IF1	IF Coarse Adjust		X	X
IF2	IF Fine Adjust		X	X
IF3	IF Coarse Adjust for L-Prime		X	X
IF4	IF Fine Adjust for L-Prime		X	X
AGC	Automatic Gain Control		X	X
VLIN	Vertical Linearity		37	10
RGBH	RGB Horizontal Shift Offset	CVBS – RGB Horizontal position compensation	8	7
VSOF	Vertical Size Offset for 60 Hz		-30	-32
VPOF	Vertical Position Offset for 60 Hz		2	1
HSOF	Horizontal Size Offset for 60 Hz		-22	-22
HPOF	Horizontal Position Offset for 60 Hz		-18	-18
HTOF	Horizontal Trap Correction Offset for 60 Hz		-19	-20
WR	White Point Adjust for RED		49	42
WG	White Point Adjust for GREEN		45	41
WB	White Point Adjust for BLUE		42	42
BR	Bias for RED		31	31
BG	Bias for GREEN		31	31

Register	Parameter	Notes	Default Values	
			A51EFS13X191	A51ELD032X001
APR	APR Threshold		10	4
BRI	Factory Setting Brightness		31	31
CON	Factory Setting Contrast		49	49
COL	Factory Setting Colour		26	26
SHA	Factory Setting Sharpness		6	6
HUE	Factory Setting Hue		31	31
VOL	Factory Setting Volume		9	9
WR-R	White Point Adjust for Red (RGB mode)		48	30
WG-R	White Point Adjust for Green (RGB mode)		53	40
WB-R	White Point Adjust for Blue (RGB mode)		37	40
FMP1	FM Prescaler when AVL is OFF	STEREO ONLY	11	11
NIP1	NICAM Prescaler when AVL is OFF	STEREO ONLY	25	25
SCP1	SCART Prescaler when AVL is OFF		11	11
SEC1	SCART Prescaler when AVL is OFF for SECAM L/L' MONO		11	11
FMP2	FM Prescaler when AVL is ON		16	16
NIP2	NICAM Prescaler when AVL is ON	STEREO ONLY	37	37
SCP2	SCART Prescaler when AVL is ON	STEREO ONLY	17	17
SEC2	SCART Prescaler when AVL is ON for SECAM L/L' MONO		17	17
F1H	High Byte of crossover frequency for VHF1-VHF3	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
F1L	Low Byte of crossover frequency for VHF1-VHF3	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
F2H	High Byte of crossover frequency for VHF3-UHF	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
F2L	Low Byte of crossover frequency for VHF3-UHF	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
BS1	Band Switch Byte for VHF1	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
BS2	Band Switch Byte for VHF3	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
BS3	Band Switch Byte for UHF	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
CB	Control Byte	Meaningful for only PLL Tuner	See "15.1 Service Registers Updating regarding the Tuner" on Page 27.	
OP1	Option 1 (see the Option List)		x	x
OP2	Option 2 (see the Option List)		x	x
OP3	Option 3 (see the Option List)		x	x
OP4	Option 4 (see the Option List)		x	x
OP5	Option 5 (see the Option List)		x	x
TX1	Teletext Option 1 (see the Option List)		x	x
GEOM	Geometry Menu		See Geometry Table on Page 25.	
OP8	Not used		x	x

14.3 Using Coloured Buttons

By using the four coloured buttons on the remote control (24, 23, 13, 14) different features or adjust may be accessed.

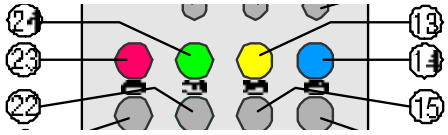


Figure 6. Coloured buttons Remote Control

14.3.1 AVL

Press the RED button (23) to activate or deactivate the AVL (Automatic Volume Level, between different broadcast channels).

14.3.2 GEOMETRY MENU

Press the GREEN button (24) in order to change from the Main Service Menu to the Geometry Menu, as shows the figure 7. To return to the Main Service Menu it should be pressed the Menu button (30), see Figure 5.

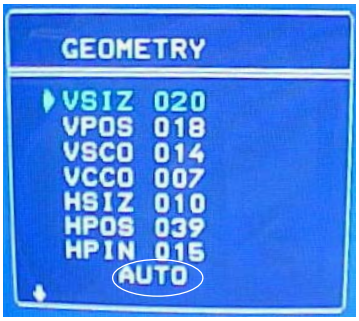


Figure 7. Geometry Menu

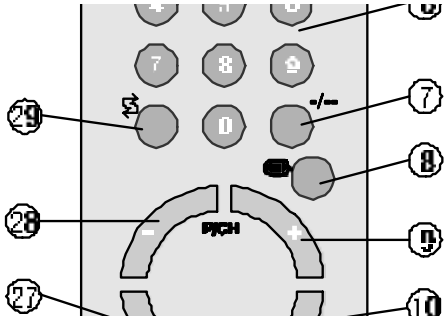


Figure 8. Remote Control

In the bottom area of this Menu, it can be seen “AUTO”. By pressing the WIDE MODE button (8) it changes to 4:3 or 16:9 format. To perform the Geometry adjustments select the most suitable option:

- AUTO, entering 4:3 or 16:9 signal and proceeding with adjustments as below.
- 4:3, entering 4:3 signal and proceeding with adjustments as below.
- 16:9, entering 16:9 signal and proceeding with adjustments as below.

14.3.2.1 Geometry Table

Register	Parameter	Default Values			
		A51EFS13X191		A51ELD032X001	
		4:3	16:9	4:3	16:9
VSIZ	Vertical Size	35	62	24	50
VPOS	Vertical Position	11	16	12	16
VSCO	Not used	14	14	14	14
VCCO	Not used	7	7	7	7
HSIZ	Not used	10	9	30	11
HPOS	Horizontal Position	33	33	40	39
HPIN	Not used	19	15	27	15
HCCO	Not used	0	0	0	0
HTRP	Not used	10	10	3	10
VZSZ	Not used	3	2	7	2

14.3.2.2 Geometry Adjustments

VSIX (Vertical Size)

Adjust the Vertical Size so that 8% over-scan is achieved.
The effect of this adjustment is shown in figure 9.

- Use the CURSOR LEFT (32) / RIGHT (3) buttons to change the data. See figure 5.

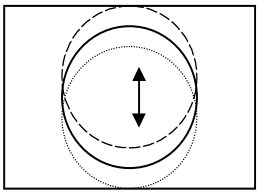


Figure 9

VPOS (Vertical Position)

Adjust the Vertical Position so that the picture is centred.
The effect of this adjustment is shown in figure 10.

- Use the CURSOR LEFT (32) / RIGHT (3) buttons to change the data. See figure 5.

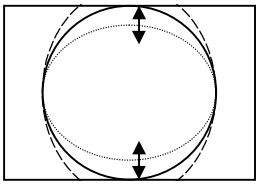


Figure 10

HPOS (Horizontal Position)

Adjust the Horizontal Position so that the picture is centred.
The effect of this adjustment is shown in figure 11.

- Use the CURSOR LEFT (32) / RIGHT (3) buttons to change the data. See figure 5.

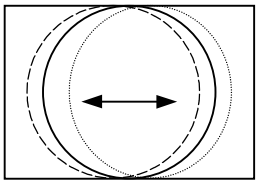


Figure 11

14.3.3 Screen Adjustment

Press the YELLOW button (13) in order to prepare the system for screen-adjustments (Vertical Scan disable). Adjust horizontal line, via screen potentiometer, as thin as possible. To return to the Main Service Menu it should be pressed the Menu button (30).

14.3.4 IF Adjustment

Select IF1, IF2, IF3 or IF4. When the blue button (14) is pressed the before selected IF register is automatically adjusted.

14.4 Auto Programming System Set Up

1. Description

In case the TV set should be serviced, there is the possibility of returning the set with the A.P.S. (Auto Programming System) activated in order to make easy the first start up to the customer. See the below figure.
If this Feature is activated the Picture and Sound Menus will be automatically memorized to the default values.

2. Before start

It is necessary let the TV set in the program number that will appear for the first time, because the A.P.S does not preset this selection.

3. Procedure

3.1 Enter the Service Mode. See Page 23.
3.2 Access to TXT1 Register by CURSOR UP / DOWN.
3.3 Press 7 button on the remote control in order to activate the Auto Programming System.
3.4 Exit the Service Mode by the Menu button (30).
3.5 Switch the TV off using the mains switch.

15. OPTION LIST

15.1 Service Registers Updating regarding the Tuner

	VHF1-VHF3 Frq. (Mhz)	VHF3-UHF Frq. (Mhz)	AK44 SERVICE MENU ITEMS							
			F1H	F1L	F2H	F2L	BS1	BS2	BS3	CB
Philips UV1316S MK3	156,25 MHz	441,25 MHz	00001100	00110010	00011110	00000010	00000001	00000010	00000100	10001110
Thomson CTT5020	114,25 MHz	401,25 MHz	00001001	10010010	00011011	10000010	00000011	00000110	10000101	10001110
Samsung TECC2949PG28B	170,25 MHz	465,25 MHz	00001101	00010010	00011111	10000010	00000001	00000010	00000100	10001110
Samsung TECC2949PG35B	170,25 MHz	449,25 MHz	00001101	00010010	00011110	10000010	00000001	00000010	00001000	10001110
Alps TEDE9X226A	142,25 MHz	425,25 MHz	00001011	01010010	00011101	00000010	00000001	00000010	00001000	10001110
Alps TEDE9-004A	149,25 MHz	424,25 MHz	00001011	11000010	00011100	11110010	00000001	00000010	00001000	10001110

Explanations	
F1H	High byte of VHF1-VHF3 cross-over frequency
F1L	Low byte of VHF1-VHF3 cross-over frequency
F2H	High byte of VHF3-UHF cross-over frequency
F2L	Low byte of VHF3-UHF cross-over frequency
BS1	Band switching byte for VHF1
BS2	Band switching byte for VHF3
BS3	Band switching byte for UHF
CB	Control byte

15.2 Registers Details

OP1 – Peripheral Options

7								NOT USED
	6							1, Display “AV-3” as “F-AV” 0, Display “AV-3” as “B-AV”
		5						1, Turn back TV mode after the last AV (with AV key) 0, Turn back first AV mode after the last AV
			4					1, SVHS is available in AV key stream 0, SVHS is NOT available in AV key stream
				3				1, RGB is available in AV key stream 0, RGB is NOT available in AV key stream
					2			1, AV-3 is available in AV key stream 0, AV-3 is NOT available in AV key stream
						1		1, AV-2 is available in AV key stream 0, AV-2 is NOT available in AV key stream
							0	0 1, AV-1 is available in AV key stream 0, AV-1 is NOT available in AV key stream

OP2 – Reception Standard Options

7							1, 3-button keyboard (V-, P+, V+) 0, 4/5 button keyboard (V-, V+, P-, P+, Menu)
	6						1, L/L’ is available 0, L/L’ is not available
		5					1, I is available 0, I is not available
			4				1, DK is available 0, DK is not available
				3			1, BG is available 0, BG is not available
					2	1	0 RESERVED (Keep as 000)

OP3 – Video Options

7	6							Xtal Configuration 00, 1 Xtal PAL 4.43 01, 2 Xtal PAL/NTSC 4.43/3.58 10, 1 Xtal PAL/SEC/NTSC 4.43 11, 2 Xtal PAL/SEC/NTSC 4.43/3.58
		5						1, Enable Blue back when no signal in AV modes 0, No blue back in AV modes
			4					1, White Insertion is ON 0, White Insertion is OFF
				3				1, Blue Background when no signal 0, Disable Blue Background
					2			1, Semi-transparent background for menu 0, Solid Menu background for menu
						1		1, Black Stretch is ON 0, Black Stretch is OFF
							0	1, APR is ON 0, APR is OFF

OP4 – TV Features

7								1, Headphone is available (for STEREO models) 0, Headphone is not available
	6							1, Arabic/Persian is Available in Menu Languages (for A, D, E, F, and later) 0, Arabic/Persian is NOT Available in Menu Languages
		5						1, Hebrew is Available in Menu Languages (for A, D, E, F, and later) 0, Hebrew is NOT Available in Menu Languages
			4					1, Hotel Mode can be activated 0, Hotel Mode can not be activated
				3				1, No Signal Timer is enabled 0, No Signal Timer is disabled
					2			For PLL Tuner 1, Frequency based search 0, Channel table based search (No meaning for VST Tuner)
						1		1, 3-band tuning (VHF1, VHF3, UHF) 0, 1-band tuning (only UHF)
							0	0 1, Extra 200 msec blanking for VST 0, no-extra blanking

OP5 – Channel Tables

7								1, Extra 150 msec blanking more for VST (if OP4.b0 = 1, to SECAM color problem) 0, no-extra blanking
	6							1, “Programme” item in AUTOSTORE menu is visible 0, “Programme” item in AUTOSTORE menu is invisible
		5						NOT USED
			4					1, French OS Channel Table is available 0, French OS Channel Table is not available
				3				1, French Channel Table is available 0, French Channel Table is not available
					2			1, England Channel Table is available 0, England Channel Table is not available
						1		1, East Europe Channel Table is available 0, East Europe Channel Table is not available
							0	1, West Europe Channel Table is available 0, West Europe Channel Table is not available

TX1 – Teletext Options

7								0, Auto Programming System off 1, Auto Programming System on
	6							RESERVED (must be 0)
		5	4	3				NOT USED
					2	1	0	Device type selection 000, EPROM M6 A 001, ROM H5 P 010, ROMLESS H5 P 011, EPROM M6 R 100, ROM M6 R 101, OSDEPROM M6 R 110, ROM M6 P 111, Read Auto Gain Table for the device from EEPROM

16. LANGUAGES

GROUP 1	GROUP 2
German	English
Italian	Polish
Dutch	Slovak
French	Hungarian
Spanish	Russian
Portuguese	Bulgarian
Swedish	Czech
Norwegian	Rumanian
Finnish	Croatian
Dannish	
English	
Greek	
Turkish	

17. HOTEL MODE FUNCTIONS

The following procedure details how to set up the Hotel Mode Functions.

1. Description

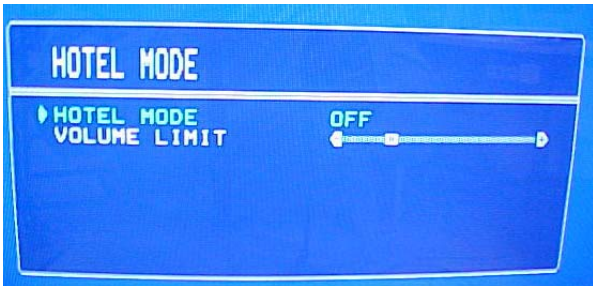
The Hotel Mode deactivates Install and Program Features from the Main Features Menu. By other hand it can be reduced the Maximum Volume Level.

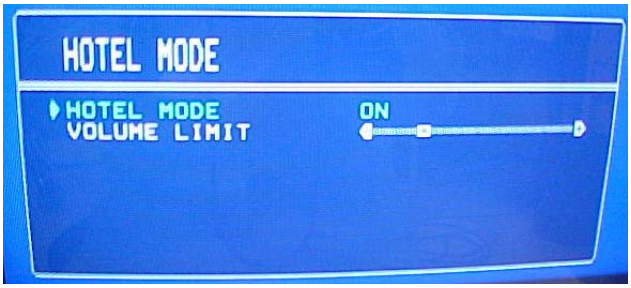
2. Before Start

It is necessary to program the channel setting (tuning and sorting) because after that this features will be deactivated.

3. Procedure

3.1 Enter the Service Mode. See Page 23.
3.2 Access to OP4 Register by CURSOR UP / DOWN.
3.3 Press 4 button on the remote control in order to activate the Hotel Mode.
3.4 Exit the Service Mode by the Menu button (30).
3.5 Enter again the Service Mode but with a new sequence of numbers: 1, 3, 2 and 5 consecutively. The following On Screen Display appears (figure on the left):

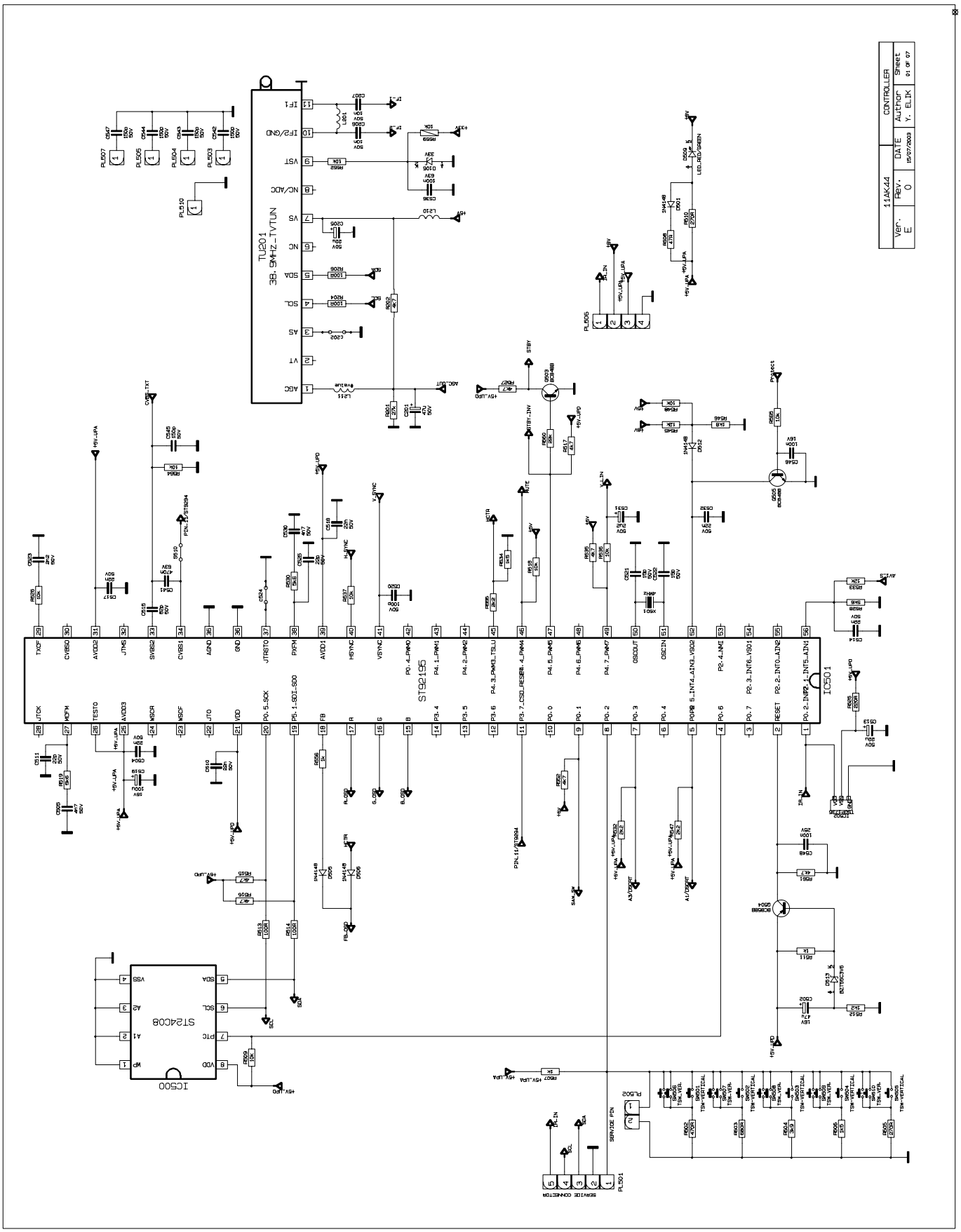




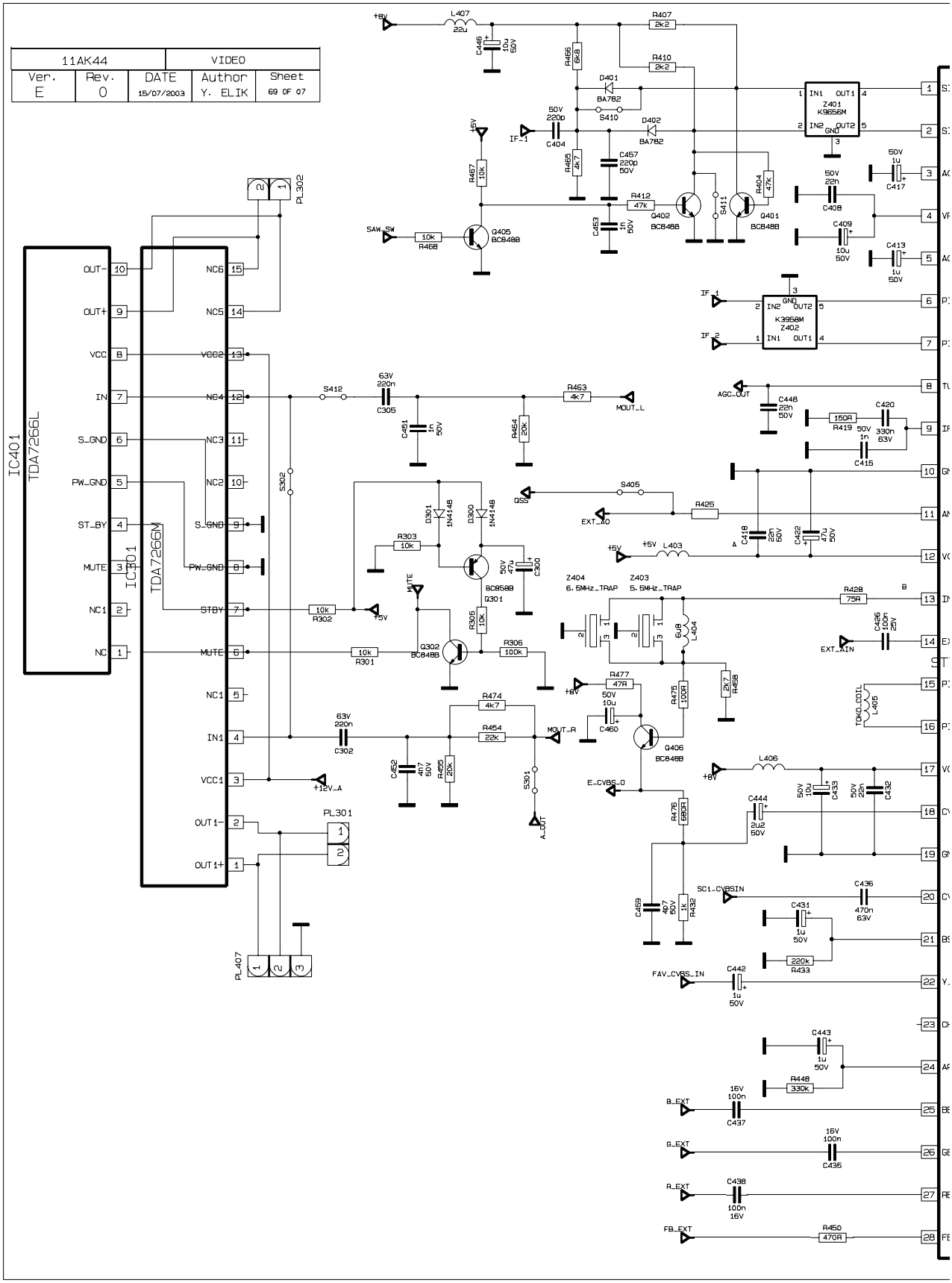
3.6 Activate the Hotel Mode as the above righ figure.
3.7 Proceed with the required Volume Limit.
3.8 Exit the Service Mode.

18. CIRCUIT DIAGRAMS

18.1 Schematic Diagram of µ-Controller & IF Circuits



18.2 Schematic Diagram of Video Circuit



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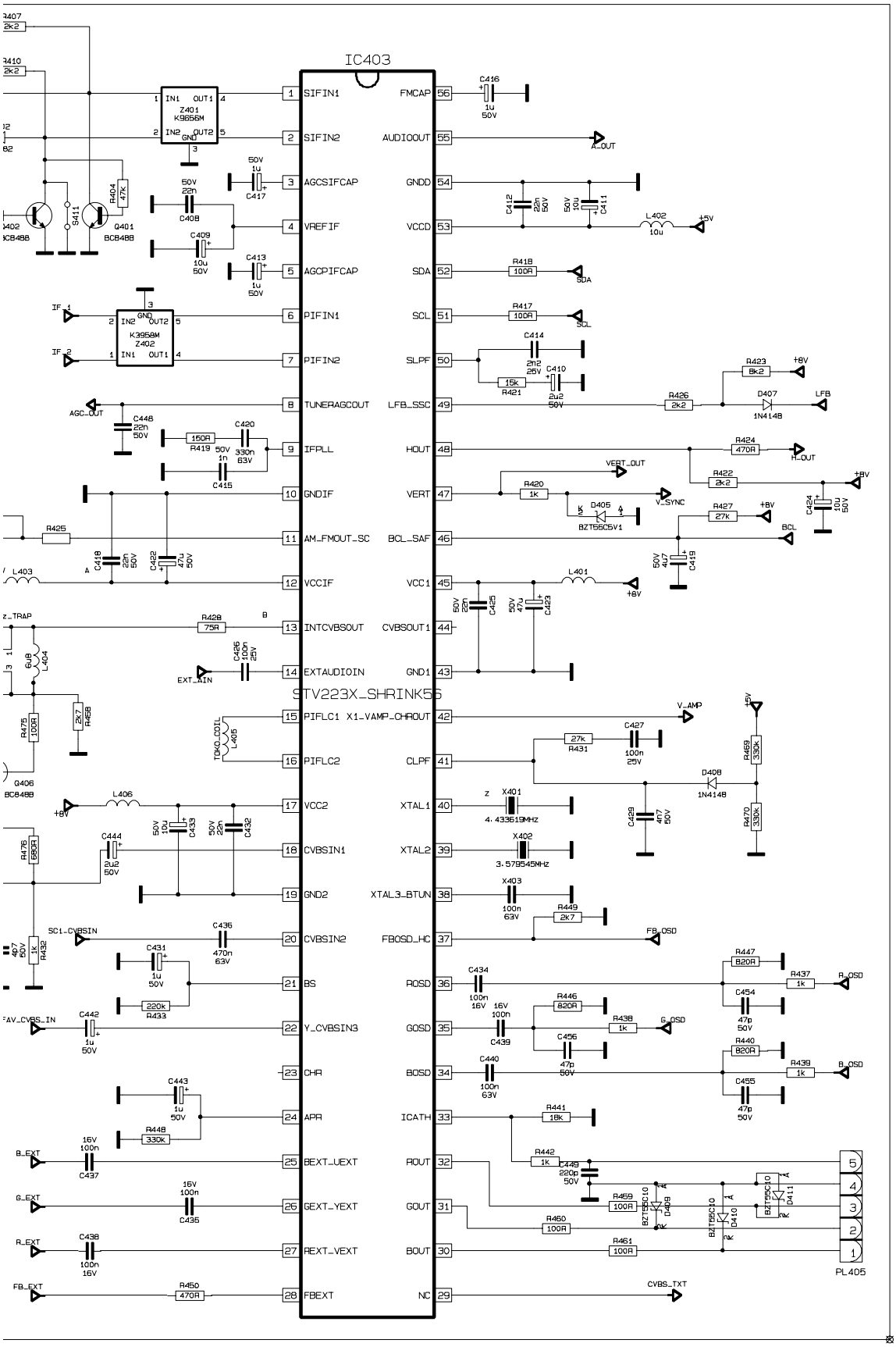
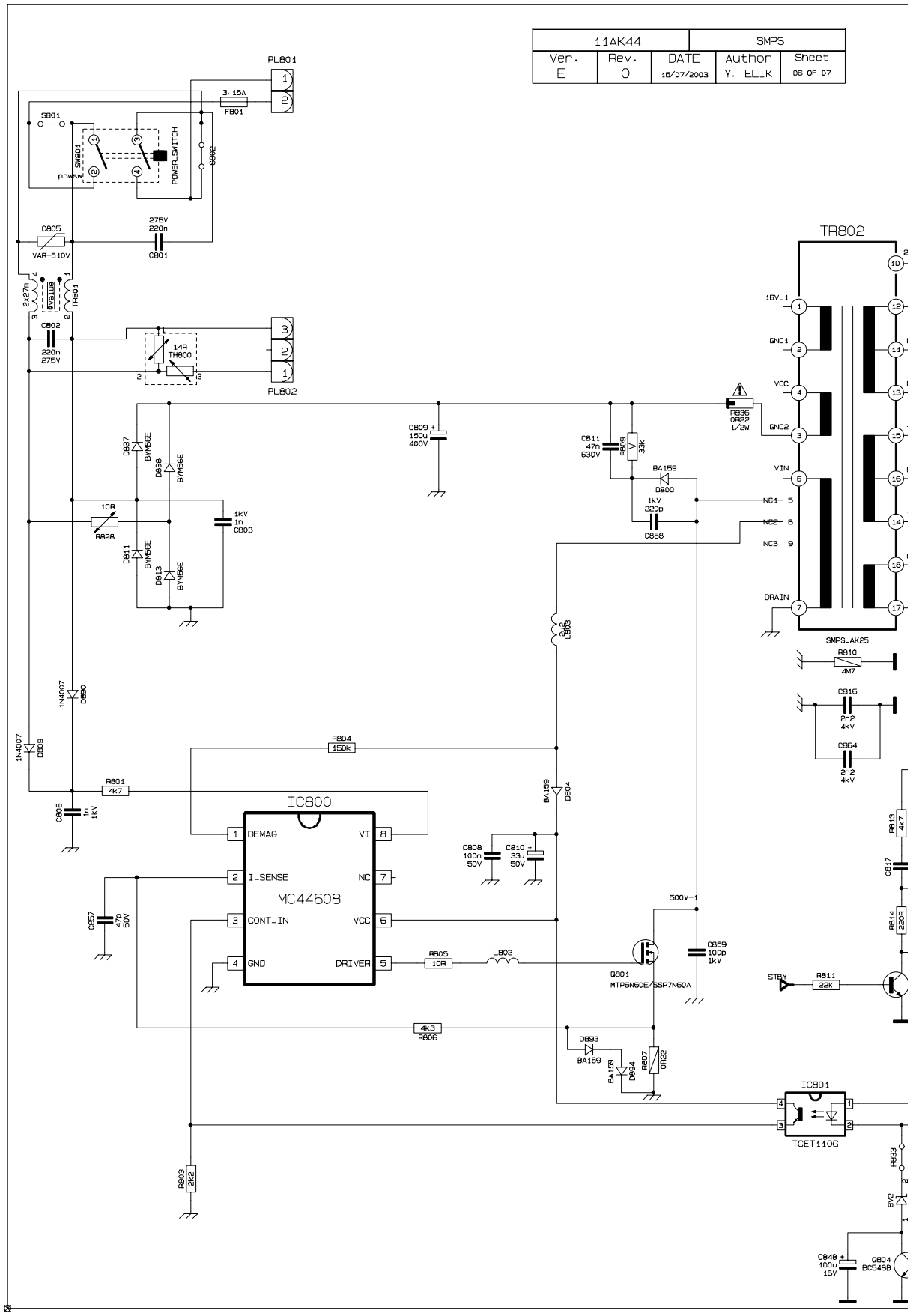
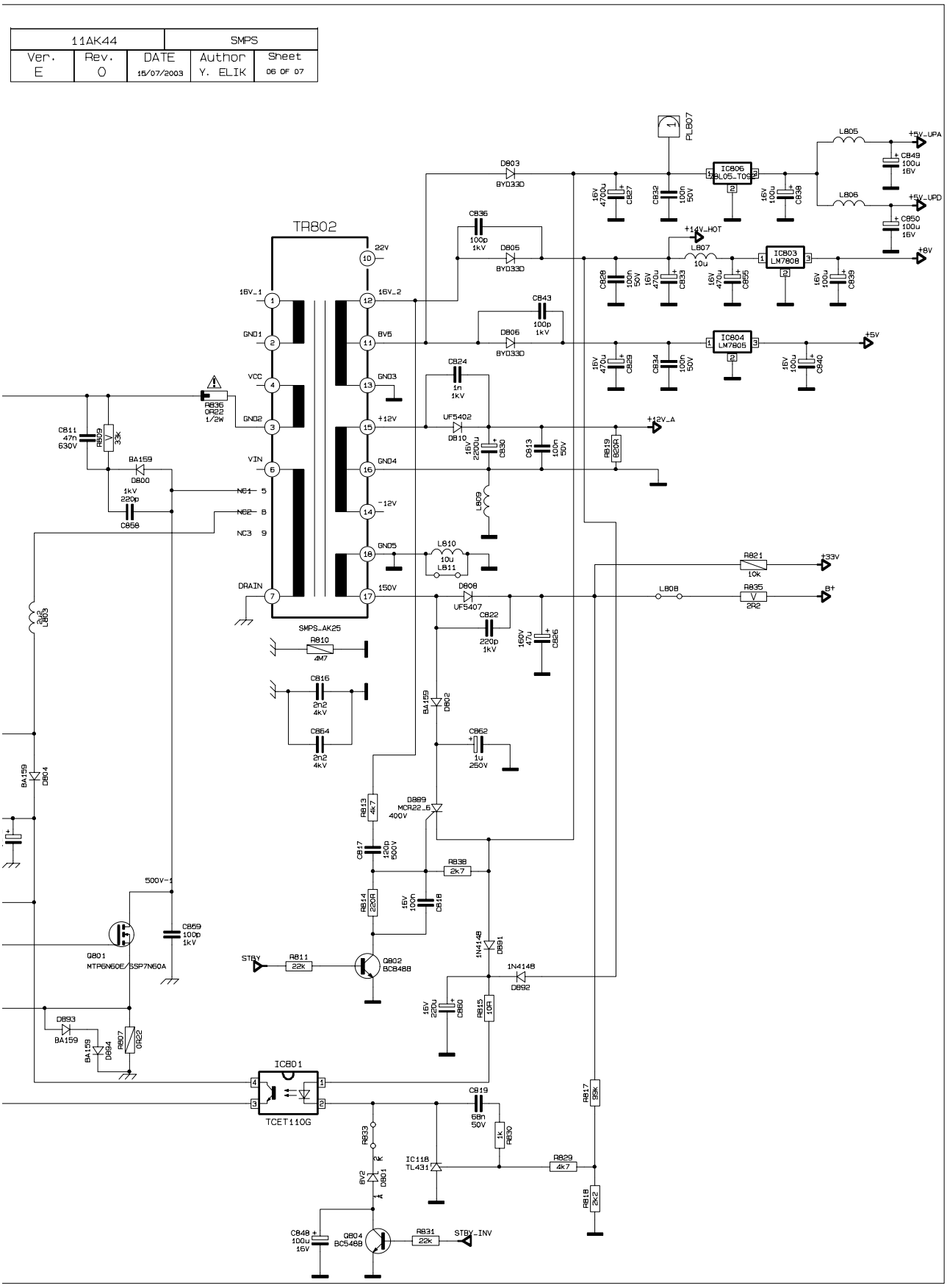
18.2 Schematic Diagram of Video Circuit



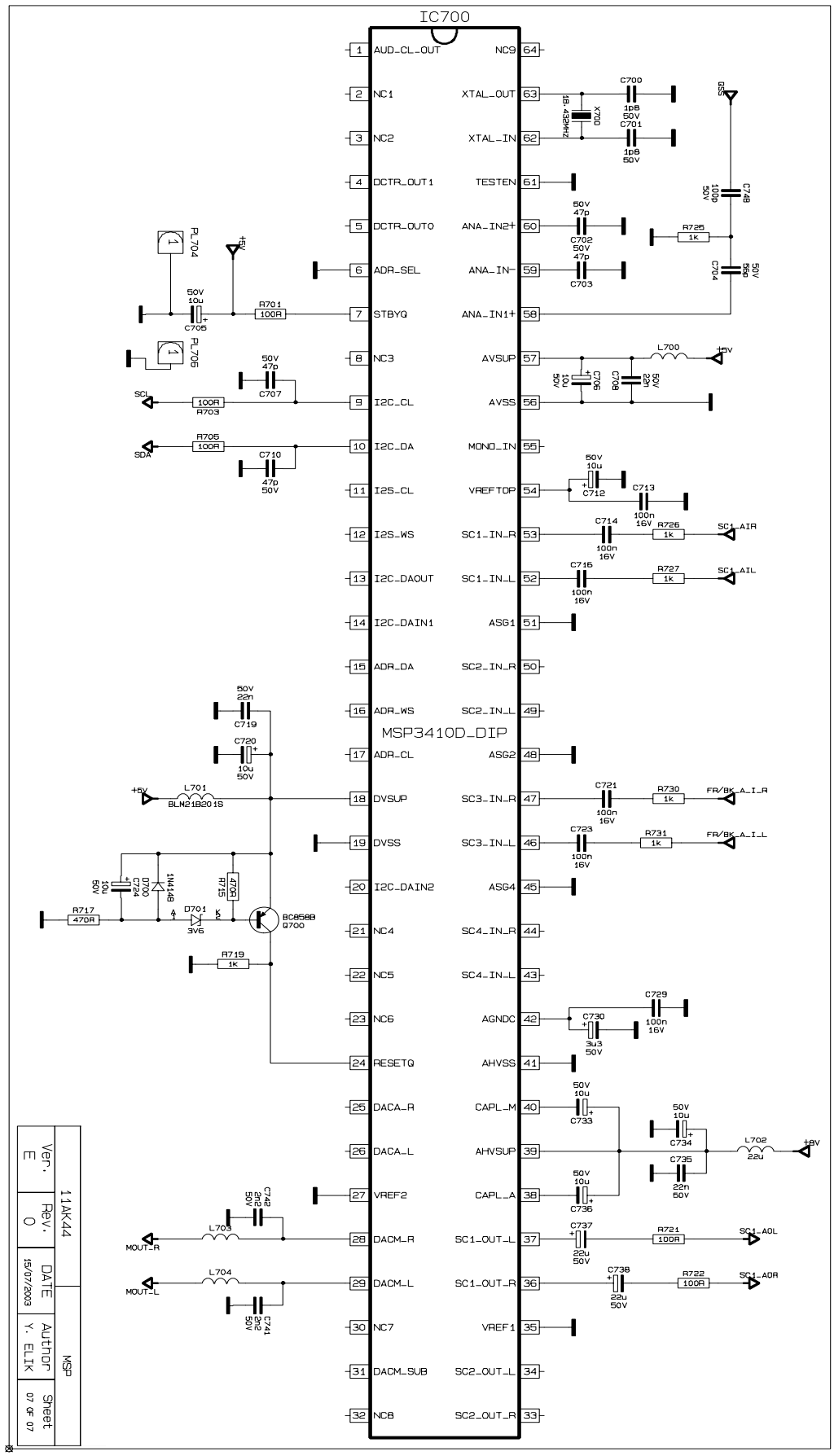
18.3 Schematic Diagram of SMPS Circuit



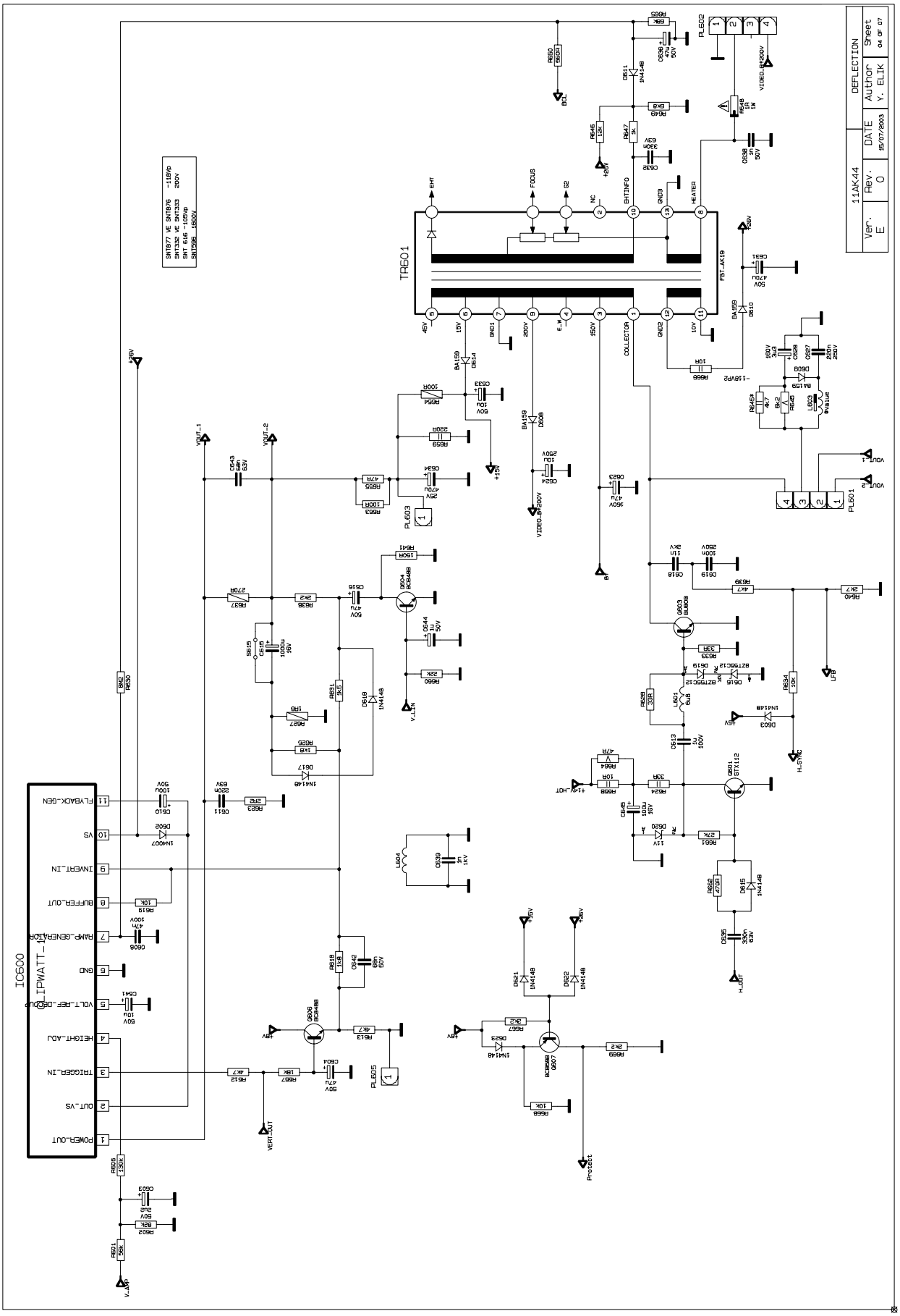
18.3 Schematic Diagram of SMPS Circuit



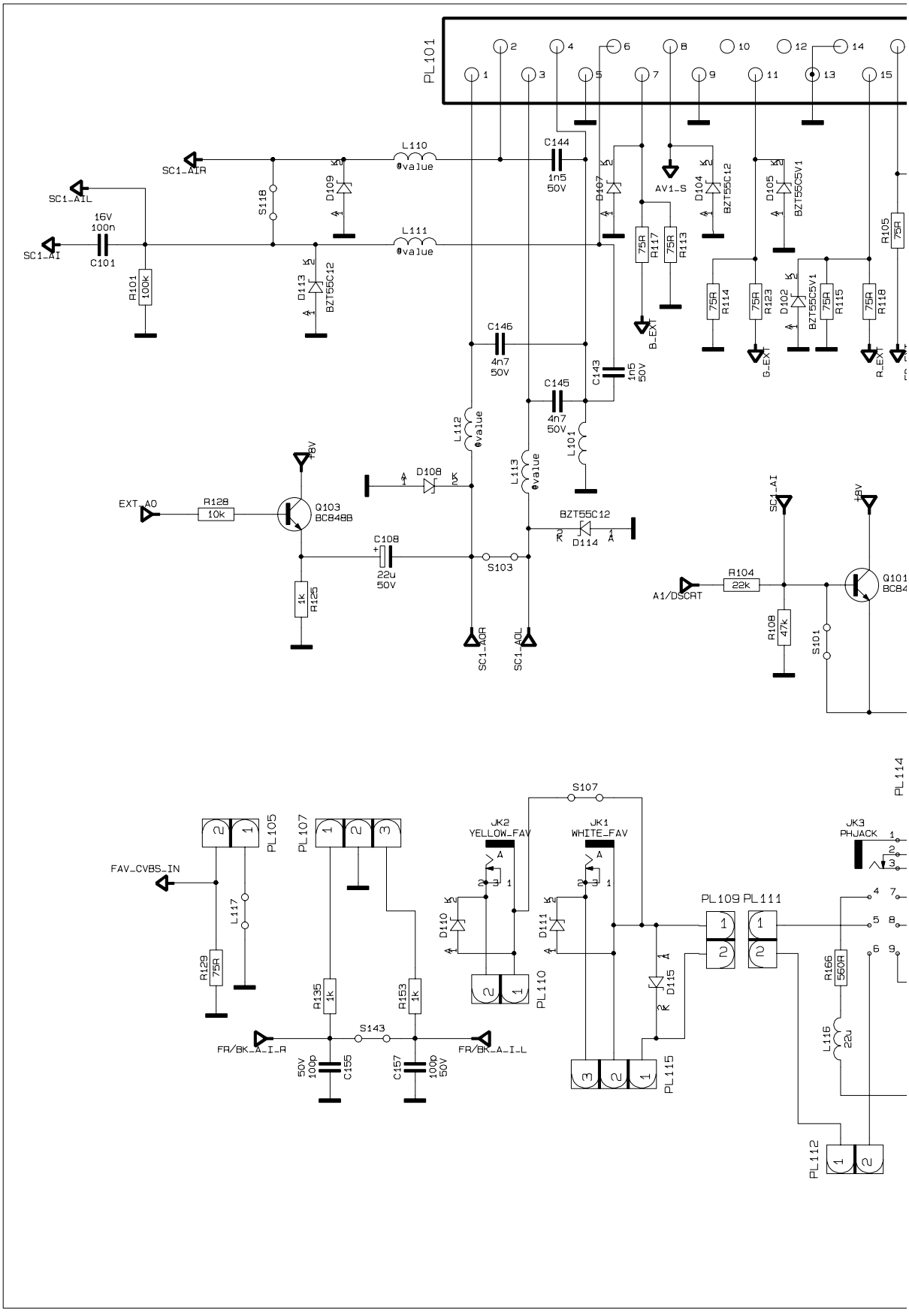
18.4 Schematic Diagram of Audio Circuit



18.5 Schematic Diagram of Deflection Circuit



18.6 Schematic Diagram of Scart & AV Front Circuits



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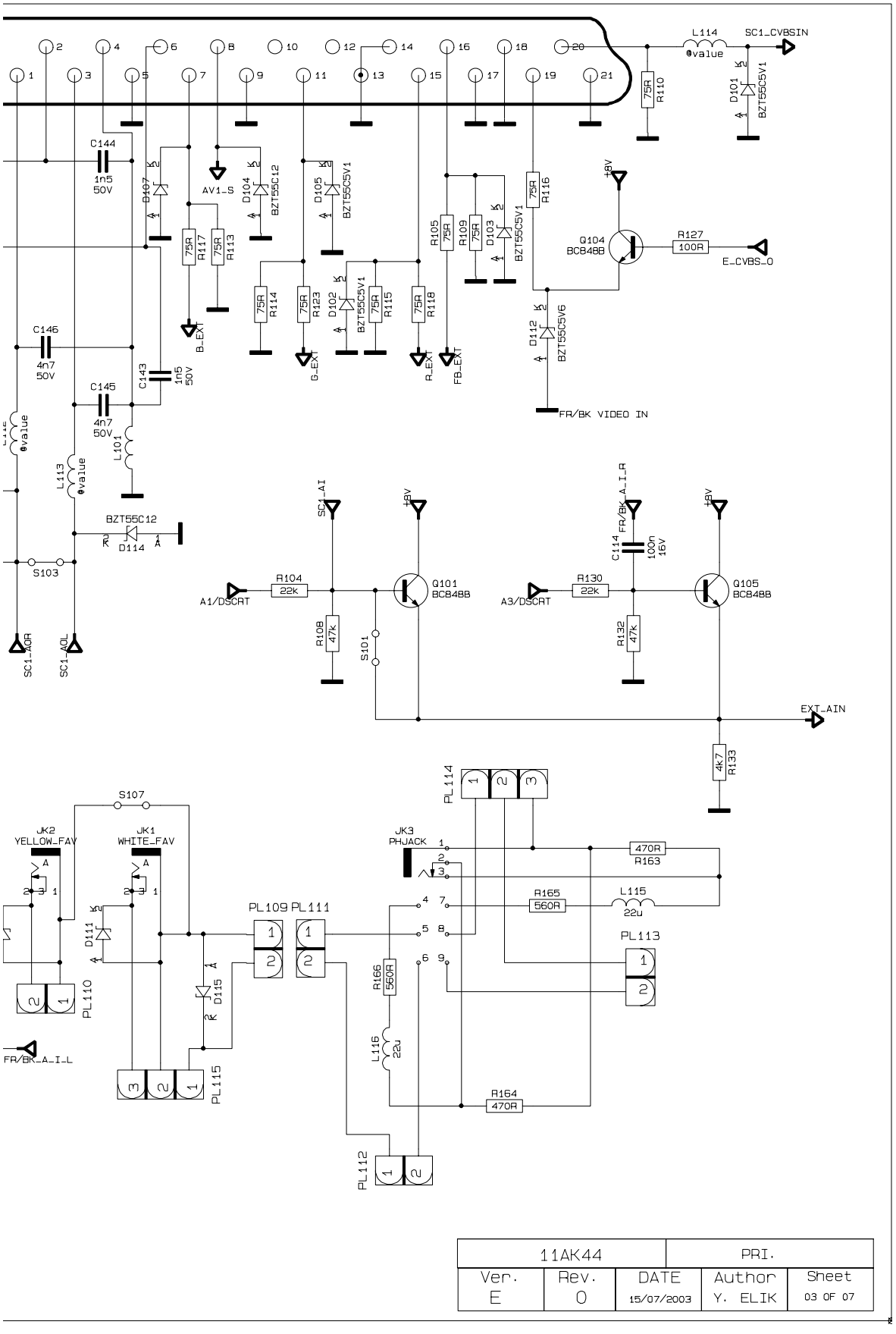
18.6 Schematic Diagram of Scart & AV Front Circuits



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Ver.	Rev.	DATE	Author	Sheet
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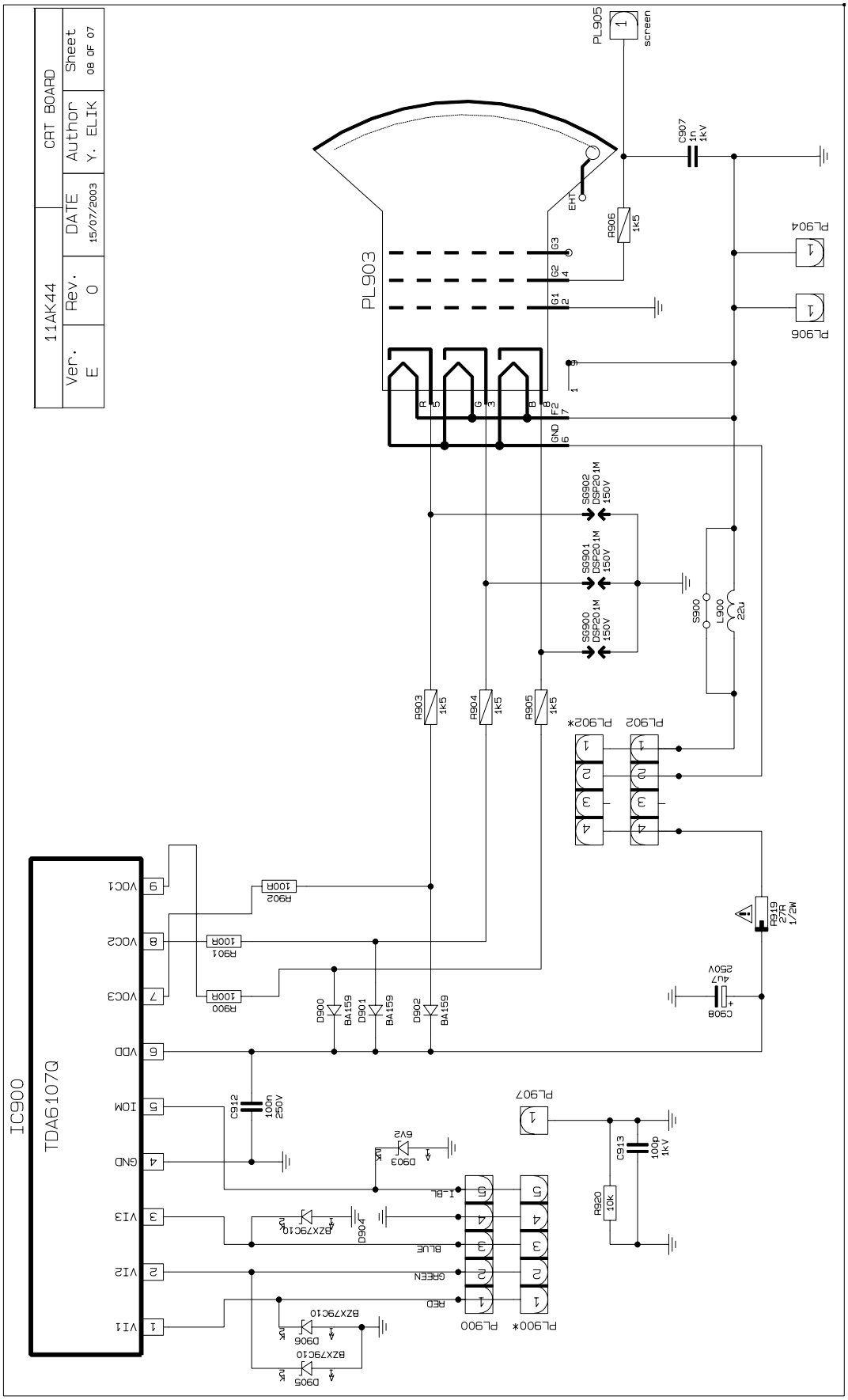
18.7 Schematic Diagram of CRT Socket Circuit



19. HOW TO UPDATE THE TECHNICAL INFORMATION

19.1 How to update the Technical Information appeared on this Service Manual (and relatives)

19.1.1. Web site: https://www.vestelservice.com

19.1.2. Select: Technical Support

19.1.3. Login: 101278

19.1.4. Password: SHPII278

By this access you can consult the latest schematic diagram or request the Parts Listing of a concrete Production Date / Serial Number.

By this way it can be also consulted the issued Technical Reports (Service Bulletins).

It can be found a Label in every chassis with additional information, i.e. the used EEPROM. See below.
On the next page are given details about the Code Bar Label.

19.2 NVM / EEPROM recorder

There is available the NVM / EEPROM recorder as spare part:

Part Reference: V20096887

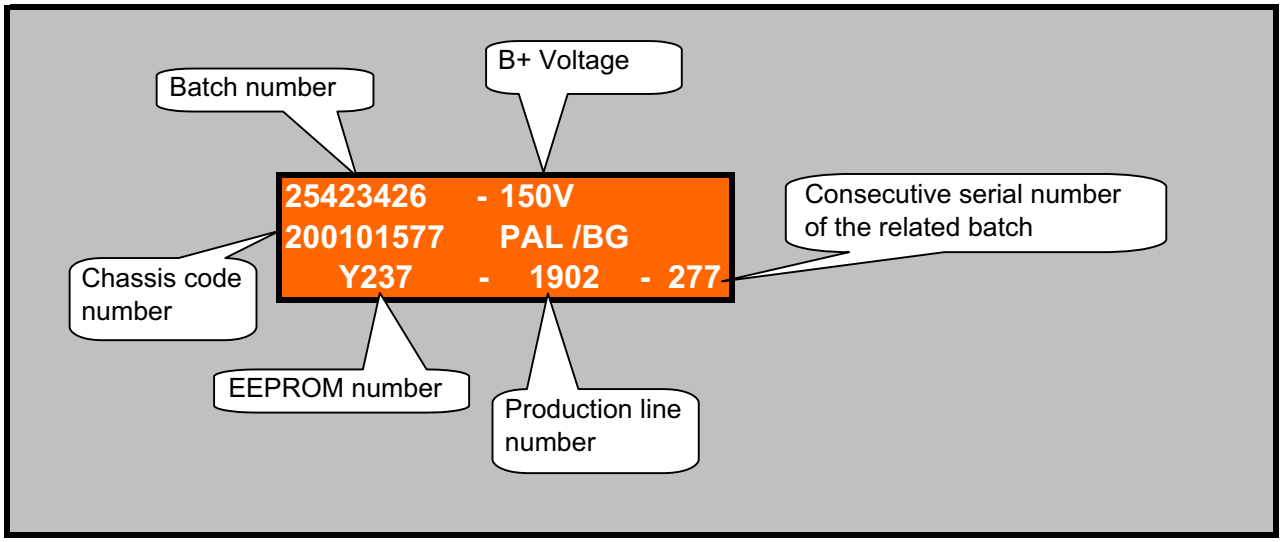
Description: MD.ASY.PONYPROG

Dom. Price Code: AT

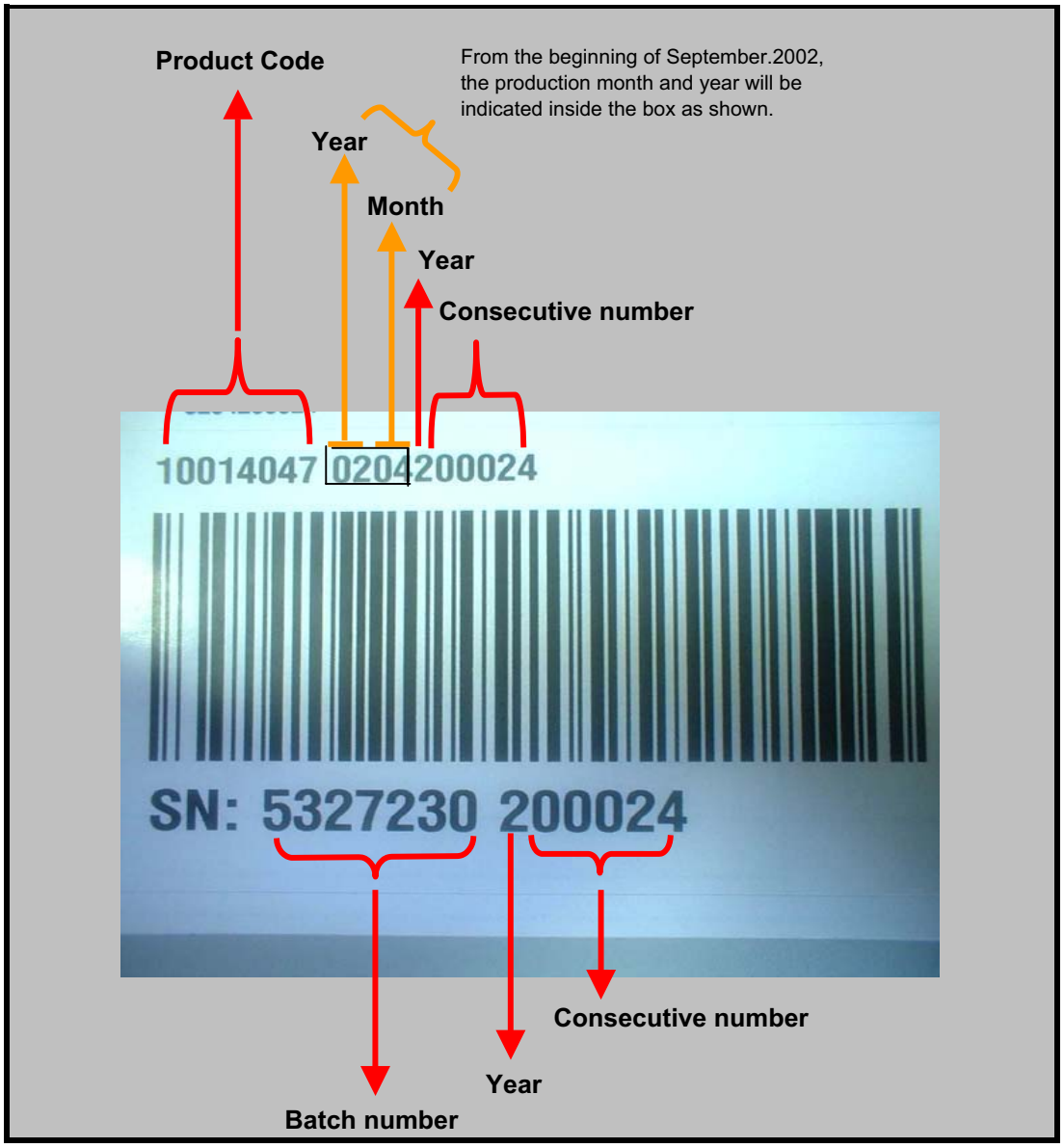
Exp. Price Code: BE

This EEPROM recorder uses the free software “Pony” available at http://www.lancos.com/ppwin95.html
Note: In case of Windows platform it is recommended the PonyProg v1.17h version.

19.3 Chassis Label Information



19.4 Code Bar Label Information



Product code:	It is the code that indicates Vestel internal identification number of the complete TV set.
Year :	Production year in two digits, e.g.: 02 for 2002
Month :	Production month in two digits; e.g.: 04 for April.
Batch number :	It is a Vestel number that is assigned by the Planning Dept. according to the customer orders. (For internal use by Vestel)
Consecutive Number:	The number that indicates the sequence of the product related to the same batch number.

Notes:

SHARP®

Technical information and Production:

Vestel Electronik AS

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